1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-05-09

SCHEM,MLB,KEPLER,2PHASE,D2

FSB, 5/9/2012

苹果笔记本维修交流群群号：325742634

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26	27	USB HUB & MUX	D2_KEPLER	01/13/2012
27	28	CPU Memory S3 Support	D2_KEPLER	01/13/2012
28	29	DDR3 SDRAM Bank A (1 OF 2)	D2_KEPLER	01/13/2012
29	30	DDR3 SDRAM Bank A (2 OF 2)	D2_KEPLER	01/13/2012
30	31	DDR3 SDRAM Bank B (1 OF 2)	D2_KEPLER	01/13/2012
31	32	DDR3 SDRAM Bank B (2 OF 2)	D2_KEPLER	01/13/2012
32	33	DDR3 Termination	D2_KEPLER	01/13/2012
33	34	DDR3/FRAMEBUF VREF MARGINING	D2_KEPLER	01/13/2012
34	35	X29/ALS/CAMERA CONNECTOR	D2_KEPLER	01/13/2012
35	36	Thunderbolt Host (1 of 2)	D2_KEPLER	01/13/2012
36	37	Thunderbolt Host (2 of 2)	D2_KEPLER	01/13/2012
37	38	Thunderbolt Power Support	D2_KEPLER	01/13/2012
38	44	RIO CONNECTOR	D2_KEPLER	01/13/2012
39	45	SSD CONNECTOR	D2_KEPLER	01/13/2012
40	46	USB 3.0 CONNECTORS	D2_KEPLER	01/13/2012
41	49	SMC	D2_KEPLER	01/13/2012
42	50	SMC Support	D2_KEPLER	01/13/2012
43	51	LPC+SPI Debug Connector	D2_KEPLER	01/13/2012
44	52	SMBus Connections	D2_KEPLER	01/13/2012
45	53	Voltage & Load Side Current Sensing	D2_SEAN	03/05/2012
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49	57	KEYBOARD/TRACKPAD (1 OF 2)	D2_KEPLER	01/13/2012
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51	59	DIGITAL ACCELEROMETER & GYRO	D2_KEPLER	01/13/2012
52	61	SPI ROM	D2_KEPLER	01/13/2012
53	62	AUDIO: CODEC/REGULATOR	D2_CARA	03/16/2012
54	63	AUDIO: HEADPHONE FILTER	D2_CARA	03/16/2012
55	64	AUDIO: IV SENSE	D2_CARA	03/16/2012
56	65	AUDIO: IV SENSE FILTER	D2_CARA	03/16/2012
57	66	AUDIO: SPEAKER AMP	D2_CARA	03/16/2012
58	67	AUDIO: JACK	D2_CARA	03/16/2012
59	68	AUDIO: JACK TRANSLATORS	D2_CARA	03/16/2012
60	69	DC-In & Battery Connectors	D2_KEPLER	01/13/2012
61	70	PBus Supply & Battery Charger	D2_KEPLER	01/13/2012
62	71	System Agent Supply	D2_KEPLER	01/13/2012
63	72	5V / 3.3V Power Supply	D2_KEPLER	01/13/2012
64	73	1V5R1V35V DDR3 SUPPLY	D2_KEPLER	01/13/2012
65	74	CPU IMVP7 & AXG VCore Regulator	D2_SEAN	03/05/2012
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67	76	CPU VCCIO (1V0R1V05 S0) POWER SUPPLY	D2_KEPLER	01/13/2012
68	77	Misc Power Supplies	D2_KEPLER	01/13/2012
69	78	Power FETs	D2_KEPLER	01/13/2012
70	79	Power Control 1/ENABLE	D2_KEPLER	01/13/2012
71	80	KEPLER PCI-E	D2_KEPLER	01/13/2012
72	81	KEPLER CORE/FB POWER	D2_SEAN	03/05/2012
73	82	KEPLER FRAME BUFFER I/F	D2_SEAN	03/05/2012
74	83	1V05 GPU / 1V35 FB POWER SUPPLY	D2_SEAN	03/05/2012
75	84	GDDR5 Frame Buffer A	D2_SEAN	03/05/2012
76	85	GDDR5 Frame Buffer B	D2_SEAN	03/05/2012
77	86	KEPLER EDP/DP/GPIO	D2_SEAN	03/05/2012
78	87	KEPLER GPIOS,CLK & STRAPS	D2_SEAN	03/05/2012
79	88	KEPLER PEX PWR/GNDS	D2_SEAN	03/05/2012
80	89	GFX IMVP VCore Regulator	D2_SEAN	03/05/2012
81	90	eDP Display Connector	D2_KEPLER	01/13/2012
82	91	eDP Mux	D2_SEAN	03/05/2012
83	92	eDP Muxed Graphics Support	D2_SEAN	03/05/2012
84	94	Thunderbolt Connector A	D2_KEPLER	01/13/2012
85	96	Thunderbolt Connector B	D2_KEPLER	01/13/2012
86	97	LCD Backlight Driver (LP8545)	D2_KEPLER	01/13/2012
87	98	PCH VCCIO (1.05V) POWER SUPPLY	D2_KEPLER	01/13/2012
88	99	Power Sequencing EG/PCH S0	D2_KEPLER	01/13/2012
89	100	CPU Constraints	D2_KEPLER	01/13/2012
90	101	Memory Constraints	D2_KEPLER	01/13/2012
91	102	PCH Constraints 1	D2_KEPLER	01/13/2012
92	103	PCH Constraints 2	D2_KEPLER	01/13/2012
93	105	Thunderbolt Constraints	D2_KEPLER	01/13/2012
94	106	SMC Constraints	D2_KEPLER	01/13/2012
95	107	GPU (Kepler) CONSTRAINTS	D2_KEPLER	01/13/2012
96	108	Project Specific Constraints	D2_CLEAN	03/15/2012
97	109	PCB Rule Definitions	D2_KEPLER	01/13/2012
98	130	DEBUG SENSORS AND ADC	D2_SEAN	03/05/2012
99	132	SMC12 SENSORS EXTENDED	D2_KEPLER	01/13/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB,KEPLER_2PHASE,D2	SCH	CRITICAL	
820-3332	1	PCBF,MLB,KEPLER_2PHASE,D2	PCB	CRITICAL	

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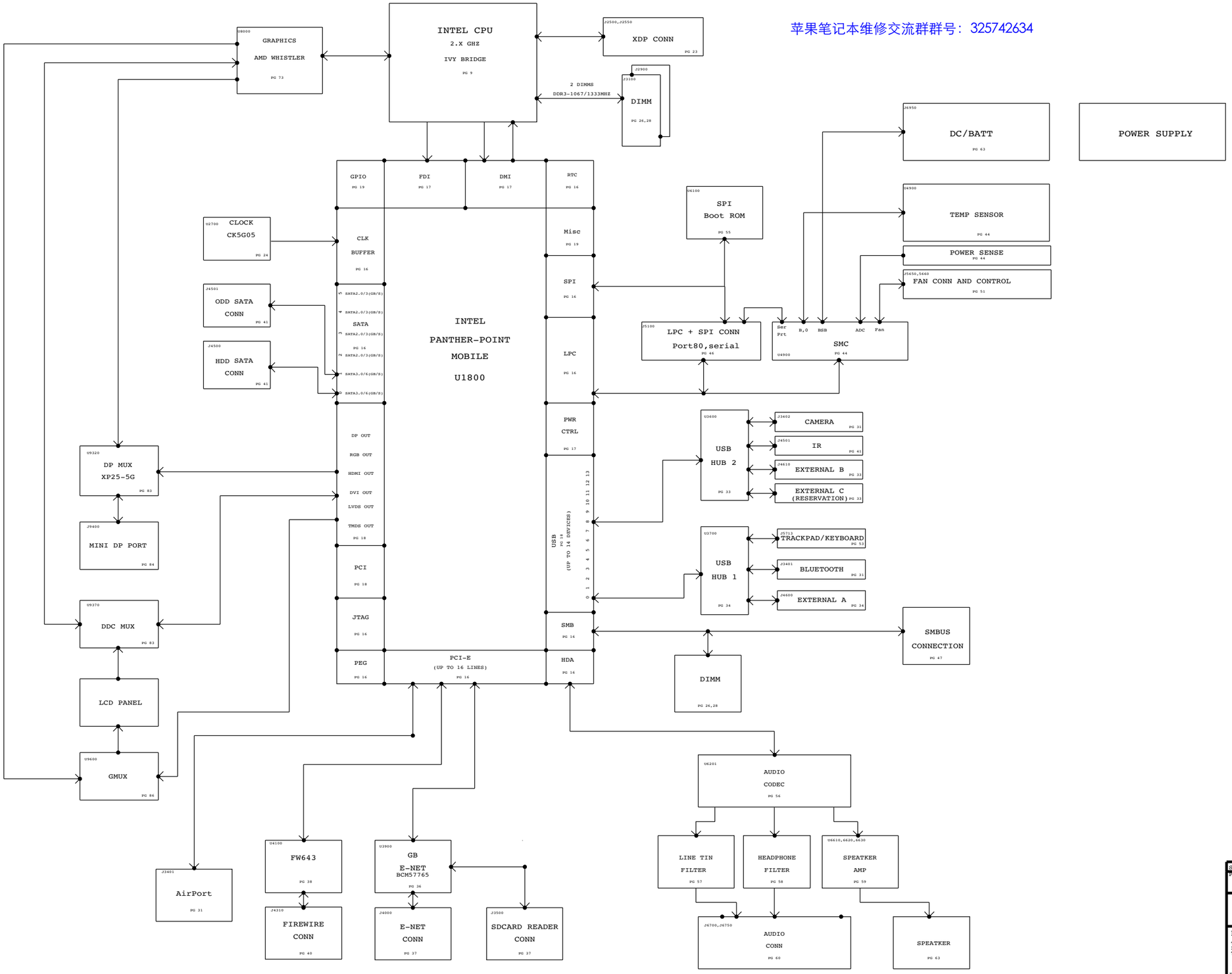

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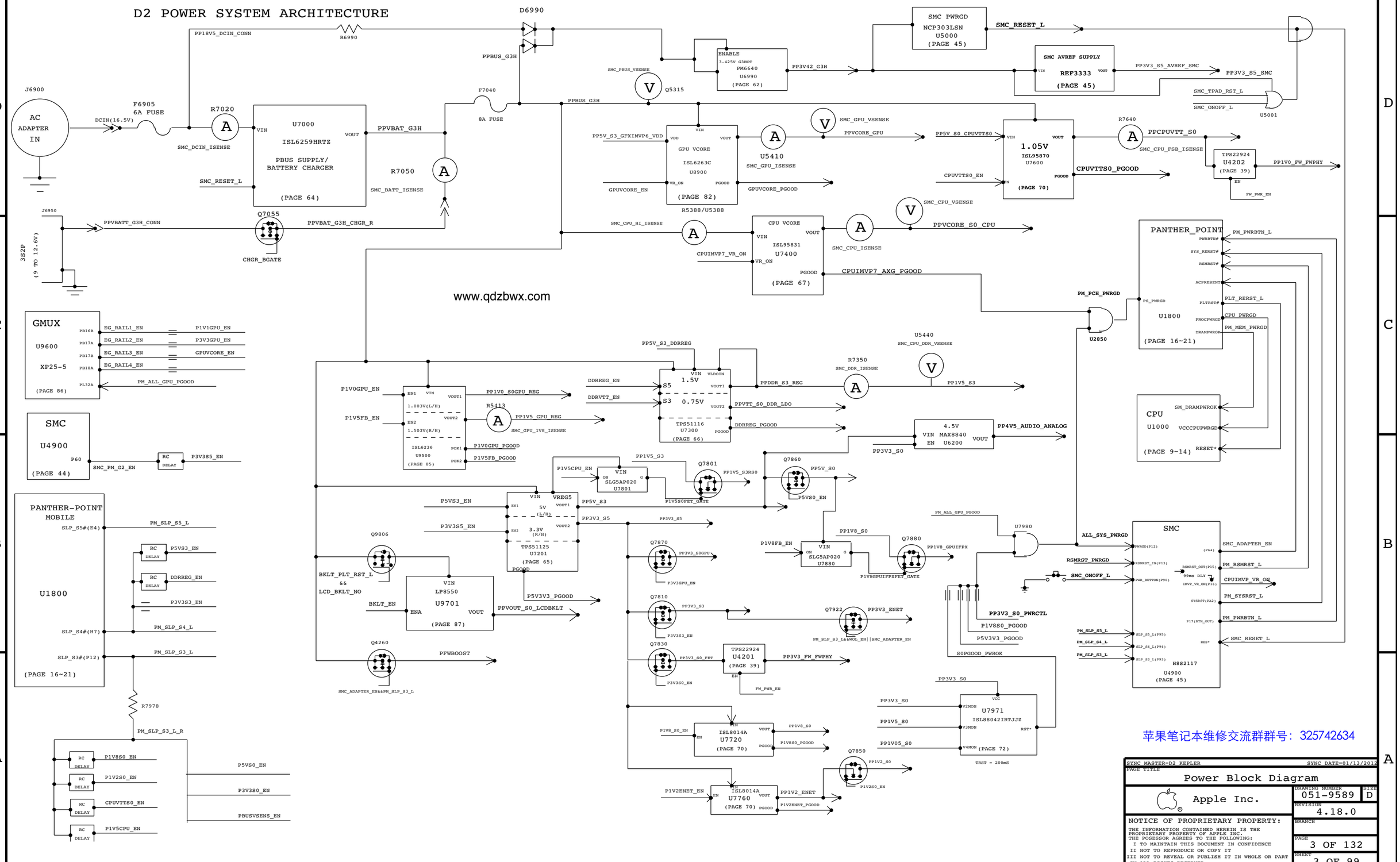
D2 POWER SYSTEM ARCHITECTURE



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BOM Variants (continued on CSA 6)

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG
085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB
607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR
685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET
685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO
639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600

BOM Groups

BOM GROUP	BOM OPTIONS
D2_COMMON	ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB
D2_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,DPMUX:HOCO,TBTRTR:PRQ,TBTBST:Y,TBTHV:P15V,HUB_2NONREM,USBHUB2512B,SPEAKERID,SMC_PACKAGE:PROD,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,P1V5S0:LDO
D2_COMMON2	EDP:YES,MIKEY,PPCPUVCCIO:IVB,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,KBD_BL:SANDWICH,CAPS:INT,BTPWR:S4,XDP,XDP_CPU:BPM,GPU:2P,TPAD_5V:LDO_S5
D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:N
D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG
D2_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,S0PGOOD_ISL,DPMUX_DEBUG,DDRVREF_DAC,VREF:ENG_M3,SENSOR_NONPROD:Y,D_BKL:DEV
D2_DEVEL:FSB	ALTERNATE,IVB_PPT_XDP
IVB_PPT_XDP	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IVB,S R0MP,PRQ,E1,2.3,45W,4+2,1.2,6M,BGA	U1000	CRITICAL	CPU_IVY:2_3GHZ
337S4267	1	IVB,S R0MM,PRQ,E1,2.6,45W,4+2,1.25,6M,BGA	U1000	CRITICAL	CPU_IVY:2_6GHZ
337S4268	1	IVB,S R0MK,PRQ,E1,2.7,45W,4+2,1.25,8M,BGA	U1000	CRITICAL	CPU_IVY:2_7GHZ
337S4269	1	PANTHER POINT,C1,SLJ8C,PRQ,BD82HM77	U1800	CRITICAL	
337S4256	1	IC,GPU,NV GK107-GTX-PS-A2	U8000	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,CIO,228 12X12 FC-CSP	U3600	CRITICAL	TBTRTR:PRQ
333S0622	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,HYNIX,C-DIE,38NM		CRITICAL	2G_HYNIX_1600
333S0623	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,SAMSUNG		CRITICAL	2G_SAMSUNG_1600
333S0628	32	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA		CRITICAL	2G_ELPIDA_1600
333S0625	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX		CRITICAL	4G_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	4G_SAMSUNG_1600
333S0629	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA		CRITICAL	4G_ELPIDA_1600
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG
128S0264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO
128S0257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET
725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL	
725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL	
806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL	
825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	

PD Parts

Bar Code Labels / EEEE #'s (continued on CSA 6)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW4]	CRITICAL	EEEE:DYW4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW5]	CRITICAL	EEEE:DYW5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT

Programmables

341S3584	1	IC,TRKPD/KYBD CNTRLR,DVB,D2	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3597	1	IC,EEPROM,CACTUS RIDGE (8.1) FSB,D2	U3690	CRITICAL	TBTROM:PROG
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPU ROM,D2,BLANK	U8701	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9100	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9100	CRITICAL	DPMUXMCU:BLANK

DRAM VREF Configs

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM
085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM
607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM
685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR

SMC

341S3308	1	IC,SMC,DEVELOPMENT-FSB,A3,D2	U4900	CRITICAL	SMC_PROG:FSB
341S3309	1	IC,SMC,PVB,A3,2.2F36,D2	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3595	1	IC,EFI,ROM,FSB, D2	U6100	CRITICAL	BOOTROM_PROG:FSB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0257	128S0264		ALL	Kemet alt to Sanyo
353S3527	353S3528		ALL	Pericom eDP MUX
353S3526	353S3528		ALL	TI eDP MUX
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0855	376S0613	VREFDQ:M1_M3	ALL	Diodes alt to Toshiba
376S1076	376S0634		ALL	Diodes alt to On Semi
376S0903	376S0796		ALL	Fairchild alt to Siliconix
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0434	197S0343		ALL	Epson Alt to TXC
197S0435	197S0343		ALL	NDK Alt to TXC
197S0432	197S0431		ALL	NDK Alt to Epson
197S0452	197S0181		ALL	Epson Alt to TXC
197S0453	197S0181		ALL	NDK Alt to TXC
685-0017	685-0016		ALL	Sanyo POSCAP/Mylar alt to Kemet
376S0975	376S1081		ALL	Toshiba alt to diodes
371S0709	371S0652		ALL	NXP alt to infineon
371S0713	371S0558		ALL	DDS alt to ST
377S0126	377S0066		ALL	New Semtech package
377S0147	377S0066		ALL	On Semi alt to Semtech
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0129		ALL	Cyntec alt to TFT
197S0466	197S0464		ALL	Epson alt to NDK
341S3564	341S3565		ALL	Avnet eDP MUX alt to Renesas

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PAGE TITLE: BOM Configuration

Apple Inc.

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REVISION: 4.18.0

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BOM Variants (continued from CSA 5)

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3382	PCBA,2.3G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DY41	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3383	PCBA,2.3G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DY42	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3445	PCBA,2.3G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DYJ5	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3446	PCBA,2.3G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DYJ6	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2818	PCBA,2.6G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRF0	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2820	PCBA,2.6G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDP	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2823	PCBA,2.6G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRDT	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2819	PCBA,2.6G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDQ	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3632	PCBA,2.7G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0JD	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3633	PCBA,2.7G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0J3	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3630	PCBA,2.7G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0J4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3631	PCBA,2.7G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0JC	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600

Bar Code Labels / EEEE #'s (continued from CSA 5)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC

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BOM Variants

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Functional Test Points

J3501 - airport

FUNC_TEST			
TRUE	AP_CLKREQ_L	34	
TRUE	AP_RESET_CONN_L	34	
TRUE	PCIE_AP_D2R_PI_N	34 92	
TRUE	PCIE_AP_D2R_PI_P	34 92	
TRUE	PCIE_AP_R2D_N	34 92	
TRUE	PCIE_AP_R2D_P	34 92	
TRUE	PCIE_CLK100M_AP_CONN_N	34 96	
TRUE	PCIE_CLK100M_AP_CONN_P	34 96	
TRUE	PCIE_WAKE_L	18 34	
TRUE	PP3V3_S3RS4_BT_F	34	
TRUE	PP3V3_WLAN	34 42	
TRUE	USB_BT_CONN_N	34 91	
TRUE	USB_BT_CONN_P	34 91	
TRUE	WIFI_EVENT_L	34 43 42	
TRUE	GND		4X GND

J3502 - ALS camera

TRUE	PP5V_S3_ALSCAMERA_F	34	
TRUE	SMBUS_SMC_2_S3_SCL	7 41 44 94	
TRUE	SMBUS_SMC_2_S3_SDA	7 41 44 94	
TRUE	USB_CAMERA_CONN_N	34 91	
TRUE	USB_CAMERA_CONN_P	34 91	
TRUE	GND		

J4400 - rio coax

TRUE	HDMI_EG_CLK_C_N	38 77 95	
TRUE	HDMI_EG_CLK_C_P	38 77 95	
TRUE	HDMI_EG_DATA_C_N<0>	38 77 95	
TRUE	HDMI_EG_DATA_C_N<1>	38 77 95	
TRUE	HDMI_EG_DATA_C_N<2>	38 77 95	
TRUE	HDMI_EG_DATA_C_P<0>	38 77 95	
TRUE	HDMI_EG_DATA_C_P<1>	38 77 95	
TRUE	HDMI_EG_DATA_C_P<2>	38 77 95	
TRUE	PCIE_CLK100M_ENET_N	17 38 92	
TRUE	PCIE_CLK100M_ENET_P	17 38 92	
TRUE	PCIE_ENET_D2R_N	17 38 92	
TRUE	PCIE_ENET_D2R_P	17 38 92	
TRUE	PCIE_ENET_R2D_C_N	17 38 92	
TRUE	PCIE_ENET_R2D_C_P	17 38 92	
TRUE	USB3_EXTB_RX_N	19 38 91	
TRUE	USB3_EXTB_RX_P	19 38 91	
TRUE	USB3_EXTB_TX_C_N	38 97	
TRUE	USB3_EXTB_TX_C_P	38 97	
TRUE	USB_EXTB_N	26 38 91	
TRUE	USB_EXTB_P	26 38 91	
TRUE	GND		19X GND

J4410 - rio flex

TRUE	ENET_CLKREQ_L	17 38	
TRUE	ENET_RESET_L	25	
TRUE	HDMI_EG_DDC_CLK	38 77	
TRUE	HDMI_EG_DDC_DATA	38 77	
TRUE	HDMI_HPD_L	38 42 82	
TRUE	I2C_DPMUX_A_SCL	44	
TRUE	I2C_DPMUX_A_SDA	44	
TRUE	PM_SLP_S3_L	7 18 27 38 41 70	
TRUE	PM_SLP_S4_L	18 27 34 38 40 41 70	
TRUE	PP1V5_S0_RIO	8	
TRUE	PP3V3_S3	7 8	3X P3V3_S3
TRUE	PP3V3_S4	7 8	
TRUE	PP5V_S4	8	5X P5V_S4
TRUE	SDCONN_STATE_CHANGE_RIO	25 38	
TRUE	SD_PWR_EN	9 38	
TRUE	USB_EXTB_OC_L	24 38	
TRUE	GND		10X GND

J5050 - hall effect

TRUE	PP3V42_G3H	7 8	
TRUE	SMC_LID_R	42	
TRUE	GND		

J5650 - left fan

TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	
TRUE	PP5V_S0	7 8	3X P5V_S0
TRUE	GND		5X GND

J5660 - right fan

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	
TRUE	PP5V_S0		3X P5V_S0
TRUE	GND		5X GND

J5815 - kbd backlight

TRUE	KBDLED_ANODE1	50	2X
TRUE	KBDLED_ANODE2	50	2X
TRUE	SMC_KBDLED_PRESENT_L	50	
TRUE	GND		4X GND

J5100 - lpc + spi

FUNC_TEST			
TRUE	LPCPLUS_GPIO	20 43	
TRUE	LPCPLUS_RESET_L	25 43	
TRUE	LPC_AD<0>	17 41 43 82 92	
TRUE	LPC_AD<1>	17 41 43 82 92	
TRUE	LPC_AD<2>	17 41 43 82 92	
TRUE	LPC_AD<3>	17 41 43 82 92	
TRUE	LPC_CLK33M_LPCPLUS	25 43 92	
TRUE	LPC_FRAME_L	17 41 43 82 92	
TRUE	LPC_PWRDWN_L	18 25 41 43	
TRUE	LPC_SERIRQ	17 41 43	
TRUE	PM_CLKRUN_L	18 41 43	
TRUE	PP5V_S0	7 8	
TRUE	SMC_RESET_L	41 42 43 61	
TRUE	SMC_ROMBOOT	42 43	
TRUE	SMC_RX_L	41 42 43	
TRUE	SMC_TCK	41 42 43	
TRUE	SMC_TDI	41 42 43	
TRUE	SMC_TDO	41 42 43	
TRUE	SMC_TMS	41 42 43	
TRUE	SMC_TX_L	41 42 43	
TRUE	SPIROM_USE_MLB	20 43 52	
TRUE	SPI_ALT_CLK	43	
TRUE	SPI_ALT_CS_L	43	
TRUE	SPI_ALT_MISO	43	
TRUE	SPI_ALT_MOSI	43	
TRUE	TP_SMC_MD1	43	
TRUE	TP_SMC_TRST_L	43	
TRUE	GND		2X GND

J5700 - ipd flex

TRUE	Z2_CS_L	49	
TRUE	Z2_DEBUG3		
TRUE	Z2_MOSI	49	
TRUE	Z2_MISO	49	
TRUE	Z2_SCLK	49	
TRUE	Z2_HOST_INTN	49	
TRUE	Z2_CLKIN	49	
TRUE	Z2_KEY_ACT_L	49	
TRUE	Z2_RESET		
TRUE	PSOC_F_CS_L	49	
TRUE	PICKB_L	49	
TRUE	PP3V3_S4	7 8	
TRUE	PP5V_S5	7 8	
TRUE	PSOC_MISO	49	
TRUE	PSOC_MOSI	49	
TRUE	PSOC_SCLK	49	
TRUE	SMBUS_SMC_2_S3_SCL	7 41 44 94	
TRUE	SMBUS_SMC_2_S3_SDA	7 41 44 94	
TRUE	GND		2X GND

J5713 - keyboard

TRUE	PP3V3_S4	7 8	
TRUE	PP3V42_G3H	7 8	
TRUE	WS_CONTROL_KBD	49	
TRUE	WS_KBD1	49	
TRUE	WS_KBD10	49	
TRUE	WS_KBD11	49	
TRUE	WS_KBD12	49	
TRUE	WS_KBD13	49	
TRUE	WS_KBD14	49	
TRUE	WS_KBD15_CAP	49	
TRUE	WS_KBD16_NUM	49	
TRUE	WS_KBD17	49	
TRUE	WS_KBD18	49	
TRUE	WS_KBD19	49	
TRUE	WS_KBD2	49	
TRUE	WS_KBD20	49	
TRUE	WS_KBD21	49	
TRUE	WS_KBD22	49	
TRUE	WS_KBD23	49	
TRUE	WS_KBD3	49	
TRUE	WS_KBD4	49	
TRUE	WS_KBD5	49	
TRUE	WS_KBD6	49	
TRUE	WS_KBD7	49	
TRUE	WS_KBD8	49	
TRUE	WS_KBD9	49	
TRUE	WS_KBD_ONOFF_L	49	
TRUE	WS_LEFT_OPTION_KBD	49	
TRUE	WS_LEFT_SHIFT_KBD	49	
TRUE	GND		2X GND

J6701 - audio flex

FUNC_TEST			
TRUE	AUD_HP_PORT_L	53 54 58	
TRUE	AUD_HP_PORT_R	53 54 58	
TRUE	AUD_SPDIF_OUT_JACK	53 58	
TRUE	AUD_TIPDET_INV	59	
TRUE	AUD_TYPEDET	58 59	
TRUE	CH_HS_GND		4X 58
TRUE	CH_HS_MIC	58	
TRUE	PP3V3_S0	7 8 96	
TRUE	US_HS_GND		4X 58
TRUE	US_HS_MIC	58	
TRUE	GND		2X GND

J6801 - 3-mic

TRUE	CON_DMIC_CLK	59	
TRUE	CON_DMIC_PWR	59	
TRUE	CON_DMIC_SDA1	59	
TRUE	CON_DMIC_SDA2	59	
TRUE	GND		

J6802 - L speaker

TRUE	SPKRCONN_L_ID	59	
TRUE	SPKRCONN_L_OUT_N	57 59 96	
TRUE	SPKRCONN_L_OUT_P	57 59 96	
TRUE	SPKRCONN_SL_OUT_N	57 59 96	
TRUE	SPKRCONN_SL_OUT_P	57 59 96	
TRUE	GND		

J6803 - R speaker

TRUE	SPKRCONN_R_ID	59	
TRUE	SPKRCONN_R_OUT_N	57 59 96	
TRUE	SPKRCONN_R_OUT_P	57 59 96	
TRUE	SPKRCONN_SR_OUT_N	57 59 96	
TRUE	SPKRCONN_SR_OUT_P	57 59 96	
TRUE	GND		

J6900 - DC PWR

TRUE	ADAPTER_SENSE	60	
TRUE	PP18V5_DCIN_FUSE	60	2X
TRUE	TDM_ONEWIRE_MPM	60	
TRUE	GND		2X GND

POWER RAILS

FUNC_TEST

TRUE	PM_SLP_S3_L	7 18 27 38 41 70
TRUE	PP0V75_S0_DDRVTT	8
TRUE	PP1V05_S0	8
TRUE	PP1V8_S0	8
TRUE	PP3V3_S0	7 8 96
TRUE	PP3V3_S0GPU	8
TRUE	PP3V3_S3	7 8
TRUE	PP3V3_S5	8 96
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	7 8
TRUE	PP5V_S0	7 8
TRUE	PP5V_S3	8
TRUE	PP5V_S5	7 8
TRUE	PPBUS_G3H	8
TRUE	PPDCIN_G3H	8
TRUE	PPVCORE_GPU	8
TRUE	PPVCORE_S0_CPU	8
TRUE	PPVTTDDR_S3	8

J6950 - battery

FUNC_TEST			
TRUE	PPVBAT_G3H_CONN		8X 60 61
TRUE	SMBUS_SMC_5_G3_SCL	41 44	
TRUE	SMBUS_SMC_5_G3_SDA	41 44	
TRUE	SYS_DETECT_L	60	
TRUE	GND		8X GND

J9000 - eDP

TRUE	DP_INT_AUX_N	81 95	
TRUE	DP_INT_AUX_P	81 95	
TRUE	DP_INT_ML_N<0>	81 95	
TRUE	DP_INT_ML_N<1>	81 95	
TRUE	DP_INT_ML_N<2>	81 95	
TRUE	DP_INT_ML_N<3>	81 95	
TRUE	DP_INT_ML_P<0>	81 95	
TRUE	DP_INT_ML_P<1>	81 95	
TRUE	DP_INT_ML_P<2>	81 95	
TRUE	DP_INT_ML_P<3>	81 95	
TRUE	LCD_FSS	81 82	
TRUE	LCD_HPD_CONN	81	
TRUE	LED_RETURN_1	81 86	
TRUE	LED_RETURN_2	81 86	
TRUE	LED_RETURN_3	81 86	
TRUE	LED_RETURN_4	81 86	
TRUE	LED_RETURN_5	81 86	
TRUE	LED_RETURN_6	81 86	
TRUE	PP5VR3V3_SW_LCD		3X 81
TRUE	PPVOUT_S0_LCDBKLT	81 86 99	
TRUE	GND		16X GND

NO_TEST=TRUE

TRUE	TBT_A_D2R_C_P<1..0>	84 93
TRUE	TBT_A_D2R_C_N<1..0>	84 93
TRUE	TBT_A_D2R_P<1..0>	7 35 84 93
TRUE	TBT_A_D2R_N<1..0>	7 35 84 93
TRUE	TBT_A_R2D_C_P<1..0>	19 7 35 84 93
TRUE	TBT_A_R2D_C_N<1..0>	35 84 93
TRUE	TBT_A_R2D_P<1..0>	84 93
TRUE	TBT_A_R2D_N<1..0>	84 93
TRUE	TBT_B_D2R_C_P<1..0>	85 93
TRUE	TBT_B_D2R_C_N<1..0>	85 93
TRUE	TBT_B_D2R_P<1..0>	35 85 93
TRUE	TBT_B_D2R_N<1..0>	35 85 93
TRUE	TBT_B_R2D_C_P<1..0>	7 35 85 93
TRUE	TBT_B_R2D_C_N<1..0>	35 85 93
TRUE	TBT_B_R2D_P<1..0>	17 85 93
TRUE	TBT_B_R2D_N<1..0>	17 85 93
TRUE	DP_TBTSNK0_ML_C_P<3..0>	35 77 95
TRUE	DP_TBTSNK0_ML_C_N<3..0>	35 77 95
TRUE	DP_TBTSNK0_ML_P<3..0>	35 95
TRUE	DP_TBTSNK0_ML_N<3..0>	35 95
TRUE	DP_TBTSNK0_AUXCH_C_P	35 83 95
TRUE	DP_TBTSNK0_AUXCH_C_N	35 83 95
TRUE	DP_TBTSNK0_AUXCH_P	49 35 95
TRUE	DP_TBTSNK0_AUXCH_N	35 95
TRUE	DP_TBTSNK1_ML_C_P<3..0>	35 77 95
TRUE	DP_TBTSNK1_ML_C_N<3..0>	35 77 95
TRUE	DP_TBTSNK1_ML_P<3..0>	35 95
TRUE	DP_TBTSNK1_ML_N<3..0>	35 95
TRUE	DP_TBTSNK1_AUXCH_C_P	35 83 95
TRUE	DP_TBTSNK1_AUXCH_C_N	35 83 95
TRUE	DP_TBTSNK1_AUXCH_P	35 95
TRUE	DP_TBTSNK1_AUXCH_N	35 95

NC NO_TESTs

		NO_TEST		
17	TP_PCIE_5_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_5_D2RN
17	TP_PCIE_5_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_5_D2RP
17	TP_PCIE_5_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_5_R2D_CN
17	TP_PCIE_5_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_5_R2D_CP
17	TP_PCIE_6_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_6_D2RN
17	TP_PCIE_6_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_6_D2RP
17	TP_PCIE_6_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_6_R2D_CN
17	TP_PCIE_6_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_6_R2D_CP
17	TP_PCIE_7_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_7_D2RN
17	TP_PCIE_7_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_7_D2RP
17	TP_PCIE_7_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_7_R2D_CN
17	TP_PCIE_7_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_7_R2D_CP
17	TP_PCIE_8_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_8_D2RN
17	TP_PCIE_8_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_8_D2RP
17	TP_PCIE_8_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_8_R2D_CN
17	TP_PCIE_8_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_8_R2D_CP
	TP_PCIE_PE5_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE5_D2RN
	TP_PCIE_PE5_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE5_D2RP
	TP_PCIE_PE5_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE5_R2D_CN
	TP_PCIE_PE5_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE5_R2D_CP
	TP_PCIE_PE6_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE6_D2RN
	TP_PCIE_PE6_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE6_D2RP
	TP_PCIE_PE6_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE6_R2D_CN
	TP_PCIE_PE6_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE6_R2D_CP
	TP_PCIE_PE7_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE7_D2RN
	TP_PCIE_PE7_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE7_D2RP
	TP_PCIE_PE7_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE7_R2D_CN
	TP_PCIE_PE7_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE7_R2D_CP
	TP_PCIE_PE8_D2RN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE8_D2RN
	TP_PCIE_PE8_D2RP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE8_D2RP
	TP_PCIE_PE8_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE8_R2D_CN
	TP_PCIE_PE8_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_PCIE_PE8_R2D_CP

PLACEABLE BEAD-PROBES FOR TBT

93 85 35 7	TBT_B_R2D_C_P<1>	TP	SM BEAD-PROBE	BP0733 SIGNAL_MODEL=EMPTY
93 85 35 7	TBT_B_R2D_C_P<0>	TP	SM BEAD-PROBE	BP0734 SIGNAL_MODEL=EMPTY
93 84 35 7	TBT_A_R2D_C_P<1>	TP	SM BEAD-PROBE	BP0735 SIGNAL_MODEL=EMPTY
93 84 35 7	TBT_A_D2R_P<1>	TP	SM BEAD-PROBE	BP0731 SIGNAL_MODEL=EMPTY
93 84 35 7	TBT_A_D2R_N<1>	TP	SM BEAD-PROBE	BP0732 SIGNAL_MODEL=EMPTY

ICT Test Points

CPU NO_TESTs

	TP_CPU_RSVD<65..62>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<65..62>
	TP_CPU_RSVD<58..45>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<58..45>
	TP_CPU_RSVD<43..32>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<43..32>
	TP_CPU_RSVD<27..26>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<27..26>
	TP_CPU_RSVD<24..15>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<24..15>
	TP_CPU_RSVD<2..1>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD<2..1>
	TP_CPU_RSVD_NCTF<8..5>	TRUE / MAKE_BASE=TRUE	NC_TP_CPU_RSVD_NCTF<8..5>

NC NO_TESTs

		NO_TEST		
18	TP_CRT_IG_BLUE	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_BLUE
18	TP_CRT_IG_GREEN	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
18	TP_CRT_IG_RED	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_RED
18	TP_CRT_IG_DDC_CLK	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
18	TP_CRT_IG_DDC_DATA	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
18	TP_CRT_IG_HSYNC	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
18	TP_CRT_IG_VSYNC	TRUE	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
18	TP_LVDS_IG_CTRL_CLK	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
18	TP_LVDS_IG_CTRL_DATA	TRUE	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
18	TP_PCH_LVDS_VBG	TRUE	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
17	TP_HDA_SDIN1	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN1
17	TP_HDA_SDIN2	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN2
17	TP_HDA_SDIN3	TRUE	MAKE_BASE=TRUE	NC_HDA_SDIN3
	TP_PCI_AD<31..0>	TRUE	MAKE_BASE=TRUE	NC_PCI_AD<31..0>
	TP_PCI_C_BE_L<3..0>	TRUE	MAKE_BASE=TRUE	NC_PCI_C_BE_L<3..0>
	TP_PCI_GNT3_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT3_L
	TP_PCI_GNT2_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT2_L
	TP_PCI_GNT1_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT1_L
	TP_PCI_GNT0_L	TRUE	MAKE_BASE=TRUE	NC_PCI_GNT0_L
	TP_PCI_PAR	TRUE	MAKE_BASE=TRUE	NC_PCI_PAR
	TP_PCI_RESET_L	TRUE	MAKE_BASE=TRUE	NC_PCI_RESET_L
	TP_PCI_PME_L	TRUE	MAKE_BASE=TRUE	NC_PCI_PME_L
	TP_PCI_CLK33M_OUT3	TRUE	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
	TP_PCH_NV_RCOMP	TRUE	MAKE_BASE=TRUE	NC_PCH_NV_RCOMP
	TP_NV_DQ<15..0>	TRUE	MAKE_BASE=TRUE	NC_NV_DQ<15..0>
	TP_NV_DQS<1..0>	TRUE	MAKE_BASE=TRUE	NC_NV_DQS<1..0>
	TP_NV_CE_L<3..0>	TRUE	MAKE_BASE=TRUE	NC_NV_CE_L<3..0>
	TP_NV_ALE	TRUE	MAKE_BASE=TRUE	NC_NV_ALE
	TP_NV_CLE	TRUE	MAKE_BASE=TRUE	NC_NV_CLE
	TP_NV_RB_L	TRUE	MAKE_BASE=TRUE	NC_NV_RB_L
	TP_NV_WR_RE_L<1..0>	TRUE	MAKE_BASE=TRUE	NC_NV_WR_RE_L<1..0>
	TP_NV_WE_CK_L<1..0>	TRUE	MAKE_BASE=TRUE	NC_NV_WE_CK_L<1..0>
	TP_PCIE_CLK100M_PE4N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
	TP_PCIE_CLK100M_PE4P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
	TP_PCIE_CLK100M_PE5N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
	TP_PCIE_CLK100M_PE5P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
	TP_PCIE_CLK100M_PE6N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
	TP_PCIE_CLK100M_PE6P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
	TP_PCIE_CLK100M_PE7N	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
	TP_PCIE_CLK100M_PE7P	TRUE	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
	TP_PSOC_P1_3	TRUE	MAKE_BASE=TRUE	NC_PSOC_P1_3
	TP_SATA_B_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_B_D2RN
	TP_SATA_B_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_B_D2RP
	TP_SATA_B_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_B_R2D_CN
	TP_SATA_B_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_B_R2D_CP
17	TP_SATA_D_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RN
17	TP_SATA_D_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_D2RP
17	TP_SATA_D_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
17	TP_SATA_D_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
17	TP_SATA_E_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RN
17	TP_SATA_E_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_D2RP
17	TP_SATA_E_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
17	TP_SATA_E_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
17	TP_SATA_F_D2RN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RN
17	TP_SATA_F_D2RP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_D2RP
17	TP_SATA_F_R2D_CN	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
17	TP_SATA_F_R2D_CP	TRUE	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
	TP_SMC_P41	TRUE	MAKE_BASE=TRUE	NC_SMC_P41

GPU NO_TESTs

		NO_TEST		
	TP_DVPDATA<21..4>	TRUE	MAKE_BASE=TRUE	NC_DVPDATA<21..4>
	TP_DVPCNTL_M<1..0>	TRUE	MAKE_BASE=TRUE	NC_DVPCNTL_M<1..0>
7	TP_DVPCNTL<2..0>	TRUE	MAKE_BASE=TRUE	NC_DVPDATA<2..0> 7
7	TP_DVPCNTL<2..0>	TRUE	MAKE_BASE=TRUE	NC_DVPDATA<2..0> 7

Thunderbolt NO_TESTs

		NO_TEST		
35	TP_TBT_XTAL25OUT	TRUE	MAKE_BASE=TRUE	NC_TBT_XTAL25OUT
35	TP_TBT_PCIE_RESET0_L	TRUE	MAKE_BASE=TRUE	NC_TBT_PCIE_RESET0_L
35	TP_TBT_PCIE_RESET1_L	TRUE	MAKE_BASE=TRUE	NC_TBT_PCIE_RESET1_L
35	TP_TBT_PCIE_RESET2_L	TRUE	MAKE_BASE=TRUE	NC_TBT_PCIE_RESET2_L
35	TP_TBT_PCIE_RESET3_L	TRUE	MAKE_BASE=TRUE	NC_TBT_PCIE_RESET3_L
35	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CP<3..0>
35	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_CN<3..0>
35	TP_DP_TBTSRC_AUXCH_CP	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CP
35	TP_DP_TBTSRC_AUXCH_CN	TRUE	MAKE_BASE=TRUE	NC_DP_TBTSRC_AUXCH_CN

PCH ALIASES

NC_LPC_DREQ0_L	MAKE_BASE=TRUE TRUE	TP_LPC_DREQ0_L	17
17 TP_CLINK_CLK	TRUE / MAKE_BASE=TRUE	NC_CLINK_CLK	
17 TP_CLINK_DATA	TRUE / MAKE_BASE=TRUE	NC_CLINK_DATA	
17 TP_CLINK_RESET_L	TRUE / MAKE_BASE=TRUE	NC_CLINK_RESET_L	
17 TP_PCIE_CLK100M_PEBN	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN	
17 TP_PCIE_CLK100M_PEBP	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP	

NC NO_TESTs

	NC_SMC_FAN_3_TACH	TRUE	
	NC_SMC_FAN_3_CTL	TRUE	
	NC_SMC_FAN_2_TACH	TRUE	
	NC_SMC_FAN_2_CTL	TRUE	
	NC_FW2_TPBP	TRUE	
	NC_FW2_TPBN	TRUE	
	NC_FW2_TPBIAS	TRUE	
	NC_FW2_TPAP	TRUE	
	NC_FW2_TPAN	TRUE	
	NC_FW0_TPBP	TRUE	
	NC_FW0_TPBN	TRUE	
	NC_FW0_TPAP	TRUE	
	NC_ESTARLDO_EN	TRUE	
	NC_ALS_GAIN	TRUE	
	NC_USB_HUB_PRTPWR2	TRUE	26
	NC_USB_HUB_PRTPWR3	TRUE	26
	NC_USB_HUB_PRTPWR4	TRUE	26
	NC_USB_HUB_OCS2	TRUE	26
	NC_USB_HUB_OCS3	TRUE	26
	NC_USB_HUB_OCS4	TRUE	26
	NC_SMC_XOSC1	TRUE	41
	NC_SMC_ODD_DETECT	TRUE	42
	NC_SMC_SYS_LED	TRUE	42
	NC_SMC_HIB_L	TRUE	41
	NC_SMBUS_SMC_4_ASF_SDA	TRUE	42
	NC_SMBUS_SMC_4_ASF_SCL	TRUE	42
	NC_SMC_T25_EN_L	TRUE	8
	NC_SMC_T25_ISENSE	TRUE	
	NC_ISNS_P1V5R1V35_CPUDDRP	TRUE	69 98
	NC_ISNS_P1V5R1V35_CPUDDRN	TRUE	69 98
	NC_ISNS_LCDBKLTP	TRUE	99
	NC_ISNS_LCDBKLTN	TRUE	99
	NC_ISNS_LCD_PANELP	TRUE	81 98
	NC_ISNS_LCD_PANELN	TRUE	81 98
	NC_ISNS_AIRPORTP	TRUE	99
	NC_ISNS_AIRPORTN	TRUE	99

	TP_HDMI_CEC	TRUE / MAKE_BASE=TRUE	NC_HDMI_CEC
	TP_DP_IG_C_HPD	TRUE / MAKE_BASE=TRUE	NC_DP_IG_C_HPD
	TP_DP_IG_C_CTRL_CLK	TRUE / MAKE_BASE=TRUE	NC_DP_IG_C_CTRL_CLK
	TP_DP_IG_C_CTRL_DATA	TRUE / MAKE_BASE=TRUE	NC_DP_IG_C_CTRL_DATA
18	TP_DP_IG_C_MLP<3..0>	TRUE / MAKE_BASE=TRUE	NC_DP_IG_C_MLP<3..0>
18	TP_D

G3H Rails

61 60 =PPBUS_G3H — PPBUS_G3H 7
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT 86
=PPVIN_S5_HS_OTHER_ISNS_R 46
=PPVIN_S5_HS_COMPUTING_ISNS_R 46
=PPVIN_S5_HS_GPU_ISNS_R 46
=PPVIN_SW_TBTBST 9 37
=PPBUS_S0_VSENSE 45
=PPBUS_G3H_T25_R

46 =PPVIN_S5_HS_COMPUTING_ISNS — PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP 65 66
=PPVIN_S3_DDRREG 64
=PPVIN_S0_CPUVCCIOS0 67
=PPVIN_S0_CPUAXG 66
=PPVIN_S0_VCCSAS0 62
=PPVIN_S0_PCHVCCIOS0 87

46 =PPVIN_S5_HS_GPU_ISNS — PPVIN_S5_HS_GPU_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S0_GFXIMVP 80
=PPVIN_S0GPU_P1V5P1V0 74

46 =PPVIN_S5_HS_OTHER_ISNS — PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.8V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3 63

60 =PP18V5_DCIN_CONN — PPDCIN_G3H 7
MIN_LINE_WIDTH=0.6 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 61

60 =PP18V5_DCIN_ISOL — PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL 61
=PPDCIN_S5_VSENSE 45

60 =PP3V42_G3H_REG — PP3V42_G3H 7
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS 43
=PP3V3_S5_SMC 41 42 78
=PP3V42_G3H_CHGR 61 70
=PP3V42_G3H_ONEWIREPROT 60
=PP3V42_G3H_PWRCTL 70
=PP3V42_G3H_SMBUS_SMC_5 44
=PP3V42_G3H_SMCUSBMUX 40
=PP3V42_G3H_TPAD 49
=PPVIN_S5_SMCVREF 42
=PPVBAT_G3_SYSCLK 25
58 =PP3V42_G3H_AUDIO
60 =PP3V42_G3H_TDM
42 =PP3V42_S3_HALL
For PCH RTC Power

25 =PPVRTC_G3_OUT — PPVRTC_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVRTC_G3_PCH 17 18 21

5V Rails

63 =PP5V_S5_LDO — PP5V_S5 7
MIN_LINE_WIDTH=0.5 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP5V_S5_P1V5S3RS0FET 69
=PP5V_S5_P5VSUSFET 69
=PP5V_S5_TPAD 49

69 =PP5V_SUS_FET — PP5V_SUS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_SUS_PCH 23

63 =PP5V_S4_REG — PP5V_S4 7
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S4_RIO 38
=PP5V_S4_P5VS0FET 69
=PP5V_S4_P5VS3FET 69
=PP5V_S0_LCD 81
=PP5V_S3_LTUSB 40
=PP5V_S4_ISNS
=PP5V_S4_TPAD 49
=PP5V_S4_AUDIO 53 59

69 =PP5V_S3_FET — PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S3_ISNS 99
=PP5V_S3_ALSCAMERA 34
=PP5V_S3_DDRREG 64
=PP5V_S3_DEBUG_ADC_AVDD 98
=PP5V_S3_DEBUG_ADC_DVDD 98
=PP5V_S3_DEBUG_ISNS 98
=PP5V_S3_MEMRESET 27

69 =PP5V_S0_FET — PP5V_S0 7
MIN_LINE_WIDTH=0.4 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
68 =PP5V_S0_P1V5_LDO
=PP5V_S0GPU_P1V0P1V35_GPU 74
=PP5V_S0_AUDIO_XW 9
=PP5V_S0_BKL 86
=PP5V_S0_CPUIMVP 65 66
=PP5V_S0_CPUVCCIOS0 67
=PP5V_S0_FAN_LT 48
=PP5V_S0_FAN_RT 48
=PP5V_S0_GFXIMVP 80
=PP5V_S0_KBDLED 50
=PP5V_S0_LPCPLUS 43
=PP5V_S0_PCH 23 25
=PP5V_S0_PCHVCCIOS0 87
=PP5V_S0_RMC 98
=PP5V_S0_VCCSAS0 62
=PP5V_S0_VMON 70

3.3V Rails

69 =PP3V3_S4_FET — PP3V3_S4 7
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
36 =PP3V3_S4_TBT_R
38 =PP3V3_S4_RIO
=PP3V3_S4_TPAD 49
=PP3V3_S4_SMC 25 42
=PP3V3_S4_BT 34

69 =PP3V3_SUS_FET — PP3V3_SUS
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V
=PP3V3_SUS_P1V05SUSLDO 68
=PP3V3_SUS_PCH_VCCSUS 21 23
=PP3V3_SUS_PCH_VCCSUS_GPIO 21 23
=PP3V3_SUS_PCH_GPIO 17 18 19 20
=PP3V3_SUS_PCH_VCCSUS_USB 21 23
=PP3V3_SUS_CNTRL 70
=PP3V3_SUS_SMC 42
52 =PP3V3_SUS_ROM
23 21 =PP3V3_SUS_PCH_VCC_SPI

63 =PP3V3_S5_REG — PP3V3_S5 7 96
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_GPU_P3V3GPUFET 69
=PP3V3_GPU_MISC_P3V3GPUMISCFET 69
=PP3V3_S0_P3V3S0FET 69
=PP3V3_S3_P3V3S3FET 69
=PP3V3_S4_DPAPWRSW
=PP3V3_S4_DPBPWRSW
=PP3V3_S4_P3V3S4FET 69
=PP3V3_S5_CPU_VCCDDR 27
=PP3V3_S5_P1V2P1V8 68
=PP3V3_S5_P1V5S0 68
=PP3V3_S5_P3V3SUSFET 69
=PP3V3_S5_PCH 18
=PP3V3_S5_PCHPWRGD 70
=PP3V3_S5_PCH_GPIO 20
=PP3V3_S5_PCH_VCCDSW 21 23
=PP3V3_S5_PWRCTL 70
=PP3V3_S5_SMCBATLOW 42
=PP3V3_S5_SYSCLK 25
=PP3V3_S5_VMON 70
=PP3V3_S5_XDP 24
=PP3V3_S4_TBTAPWRSW 84
=PP3V3_S4_TBTBPWRSW 85

69 =PP3V3_S3_FET — PP3V3_S3 7
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S3_BT 34
=PP3V3_S3_DPMUX_UC 82
=PP3V3_S3_ISNS 99
=PP3V3_S3_MEMRESET 27
=PP3V3_S3_PCH_GPIO 19 25
=PP3V3_S3_RIO 38
=PP3V3_S3_SMBUS_SMC_2_S3 44
=PP3V3_S3_SMBUS_SMC_3 44
=PP3V3_S3_TPAD
=PP3V3_S3_USBMUX 26
=PP3V3_S3_USB_HUB 26
=PP3V3_S3_USB_RESET 26
=PP3V3_S3_VREFMRGN 33
=PP3V3_S3_WLAN 34
=PP3V3_S3_GYRO 51
=PP3V3_S3_SMS 51
=PP3V3_S3_SDBUF 25

69 =PP3V3_S0_FET — PP3V3_S0 7 96
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 mm MAKE_BASE=TRUE
=PP3V3_S0_AUDIO 59
=PP3V3_S0_AUDIO_DIG 53 58
=PP3V3_S0_BKL_VDDIO 86
=PP3V3_S0_CPUTHMSNS 47
=PP3V3_S0_CPU_VCCIO_SEL 13
=PP3V3_S0_DPMUX 82 83
=PP3V3_S0_DPMUXI2C 44
=PP3V3_S0_DPMUX_UC 35 78 82
=PP3V3_S0_FAN_LT 48
=PP3V3_S0_FAN_RT 48
=PP3V3_S0_GPUTHMSNS 47
=PP3V3_S0_HS_ISNS 46
=PP3V3_S0_IMVPISNS 46
=PP3V3_S0_ISNS 45 98 99
=PP3V3_S0_LCD 81
=PP3V3_S0_P1V8GPUFET
=PP3V3_S0_P3V3TBTFET 37
=PP3V3_S0_PCH 17 23
=PP3V3_S0_PCH_GPIO 17 18 19 20 25 37
=PP3V3_S0_PCH_VCC3_3_CLK 23
=PP3V3_S0_PCH_VCC3_3_GPIO 21 23
=PP3V3_S0_PCH_VCC3_3_HVCMOS 21 23
=PP3V3_S0_PCH_VCC3_3_PCI 21 23
=PP3V3_S0_PCH_VCC3_3_SATA 21 23
=PP3V3_S0_PCH_VCCADAC 23
=PP3V3_S0_PWRCTL 70 88
=PP3V3_S0_RSTBUF 25
=PP3V3_S0_SATAMUX 39
=PP3V3_S0_SB_PM 25 70
=PP3V3_S0_SMBUS_PCH 44
=PP3V3_S0_SMBUS_SMC_0_S0 44
=PP3V3_S0_SMBUS_SMC_1_S0 44
=PP3V3_S0_SSD 39
=PP3V3_S0_SYSCLK 25
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL 37
=PP3V3_S0_TPAD 50
=PP3V3_S0_VMON 70
=PP3V3_S0_X29THMSNS 47
=PP3V3_S0_XDP 24
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS

TBT RAILS

37 =PP3V3_TBTLC_FET — PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V MIN_NECK_WIDTH=0.15 MM
MAKE_BASE=TRUE
=PP3V3_TBT_PCH_GPIO 20
=PPVDDIO_TBT_CLK 25
=PP3V3_TBTLC_RTR 35 36 37

37 =PP1V05_TBTLC_FET — PP1V05_TBTLC 37
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTLC_RTR 36

37 =PP1V05_TBTCIO_FET — PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTCIO_RTR 36

37 9 =PP15V_TBT_REG — PP15V_TBT
MIN_LINE_WIDTH=0.4 MM VOLTAGE=15V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPHV_SW_TBTAPWRSW 84
=PPHV_SW_TBTBPWRSW 85

1.8V/1.5V/1.2V/1.05V Rails

68 =PP1V8_S0_REG — PP1V8_S0 7
4A max supply
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM 21
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL 15
=PP1V8_S0_GPUFET
=PP1V8_S0_PCH_VCCTX_LVDS 23
=PP1V8_S0_PCH_VCC_DFTERM 20 21 23
=PPVDDIO_S0_SBCLK 25
=PP1V8_S0_P1V5_LDO 68

15 13 =PP1V8_S0_CPU_VCCPLL_R — PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

64 =PPDDR_S3_REG — PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET 27
=PPDDR_S3_MEMVREF 33
=PPVIN_S3_P1V5S3RS0_FET 69
=PPVIN_S0_DDRREG_LDO 64
=PPVIN_S3_MEM_ISNS_R 45

45 =PPVIN_S3_MEM_ISNS — PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A 28 29
=PP1V5R1V35_S3_MEM_B 30 31

69 =PP1V5_S3RS0_FET_ISNS — PP1V5_S3RS0_CPUDDR 96
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3RS0_VMON 70
=PP1V5_S3_CPU_VCCDDR 11 14 16 27

68 =PP1V5_S0_REG — PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_AUDIO 53
=PP3V3R1V5_S0_PCH_VCCSUSHDA 21 23 25

68 =PP1V5_S0_RIO_LDO — PP1V5_S0_RIO 7
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V5_S0_RIO 38

64 33 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

64 =PPVTT_S0_DDR_LDO — PP0V75_S0_DDRVTT 7
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A 32
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 27

68 =PP1V05_SUS_LDO — PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG 24

67 =PPCPUVCCIO_S0_REG — PP1V05_S0 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU_VCCIO 10 11 13 14 15
=PPVCCIO_S0_XDP 24
=PPVCCIO_S0_CPUIMVP 65
=PPVCCIO_S0_SMC 42
=PP1V05_S0_VMON 70
=PP1V05_S0_RMC 98

87 =PPPCHVCCIO_S0_REG — PP1V05_PCHVCCIO_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE 21
=PP1V05_S0_PCH_VCCADPLL 23
=PP1V05_S0_PCH_VCCIO 21 23
=PP1V05_S0_PCH_VCCIO_PCIE 18
=PP1V05_S0_PCH_VCCIO_SATA 17 21 23
=PP1V05_S0_PCH_VCCIO_CLK 8 21 23
=PP1V05_S0_PCH_VCCIO_USB 21 23
=PP1V05_S0_PCH_VCC_CORE 21 23
=PP1V05_S0_PCH_VCCASW 21 23
=PP1V05_S0_PCH_VCCIO_CLK 8 21 23
=PP1V05_S0_PCH_VCCDIFFCLK 17 21 23
=PP1V05_S0_PCH 17 23
=PP1V05_S0_PCH_VCCSSC 21 23
=PP1V05_S0_PCH_V_PROC_IO 21 23
=PP1V05_S0_PCH_VCCIO_PLLUSB 21
=PP1V05_S0_PCH_VCC_DMI 21 23
=PP1V05_S0_PCH_VCCIO_PLLFDI 21
=PP1V05_S0_PCH_VCCDMI_FDI 21
=PP1V05_S0_P1V05TBTFET_R 99

Defined here since TBT page does not know PBUS voltage
I167 PPVIN_SW_TBTBST 37
VOLTAGE=12.8V

Backlight Rails

99 =PPBUS_SW_BKL — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.6V
PPBUS_S0_LCDBKLT_PWR 86

41 SMC_T25_EN_L — NC_SMC_T25_EN_L 7
MAKE_BASE=TRUE

99 37 =PP1V05_S0_P1V05TBTFET — PP1V05_S0_P1V05TBTFET
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

"GPU" Rails

88 69 =PP3V3_S0GPU_FET — PP3V3_S0GPU 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_IFPX_PLLVDD 77
=PP3V3_S0_GFX3V3BIAS 80
=PP3V3_GPU_VDD33 71 77 78 79

69 =PP3V3_S0GPU_MISC_FET — PP3V3_S0GPU_MISC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_MISC 77

TP_P1V8GPU_EN — =P1V8GPU_EN 88

74 =PP1V5R1V35_GPU_REG — PP1V5R1V35_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V35_GPU_FBVDDQ 72 75 76
=PP1V35_GPU_S0_FB 73

88 =PP1V8_GPU_FET — TP_GPU_PGOOD2
MAKE_BASE=TRUE

74 =PP1V05_S0GPU_REG — PP1V0_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V0_GPU_DPLL
=PP1V0_GPU_DP_AB
=PP1V0_GPU_DP_CD
=PP1V05_GPU_IFPCD_IOVDD 77
=PP1V05_GPU_IFPEF_IOVDD 77
=PP1V05_GPU_PEX_IOVDD 73 79
=PP1V05_GPU_PEX_PLLVDD 77 79

45 =PPVCORE_GPU_REG — PPVCORE_GPU 7
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.0V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCORE_GPU 72 79
=PPVCORE_S0_GFX_REG 80

GND — =LVDS_VCCA 21
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.085MM
VOLTAGE=0V
MAKE_BASE=TRUE

Chipset "VCore" Rails

66 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU 7
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 MM VOLTAGE=1.25V
=PPVCORE_S0_CPU 13 15 45 98

66 45 =PPVCORE_S0_AXG_REG — PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
=PPVCORE_S0_CPU_VCCAXG 13 14 16

16 13 =PP1V5_S3_CPU_VCCDQ — PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.5V

15 13 =PP1V05_S0_CPU_VCCPOE — PP1V05_S0_CPU_VCCPOE
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

99 62 =PPVCCSA_S0_REG — PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 MM VOLTAGE=0.9V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCCSA_S0_CPU 13 16

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Frame Holes

ZT0915 2.8R2.3 — GND_BATT_CHGND
ZT0950 TH-NSP — GND_CHASSIS_FAN — SL-2.3X3.9-2.9X4.5
ZT0974 TH-NSP — GND_CHASSIS_MLBCAN5 — SL-1.1X0.45-1.4x0.75
ZT0975 TH-NSP — GND_CHASSIS_MLBCAN6 — SL-1.1X0.45-1.4x0.75
GND MAKE_BASE=TRUE

ZT0970 TH-NSP — GND_CHASSIS_MLBCAN1 — SL-1.1X0.45-1.4x0.75
ZT0971 TH-NSP — GND_CHASSIS_MLBCAN2 — SL-1.1X0.45-1.4x0.75
ZT0972 TH-NSP — GND_CHASSIS_MLBCAN3 — SL-1.1X0.45-1.4x0.75
ZT0973 TH-NSP — GND_CHASSIS_MLBCAN4 — SL-1.1X0.45-1.4x0.75

THERMAL MODULE STANDOFFS

SH0920 STDOFF-4.5OD2.15H-SM
SH0927 STDOFF-4.5OD2.15H-SM
SH0926 STDOFF-4.5OD2.15H-SM
SH0925 STDOFF-4.5OD1.8H-SM
SH0928 STDOFF-4.5OD2.15H-SM
SH0921 STDOFF-4.5OD2.15H-SM-1
SH0929 STDOFF-4.5OD2.15H-SM
SH0923 STDOFF-4.5OD1.8H-SM
SH0922 STDOFF-4.5OD2.15H-SM
SH0930 STDOFF-4.5OD2.15H-SM
SH0924 STDOFF-4.5OD1.9H-SM
SH0946 STDOFF-4.9OD2.38H-SM-2
SH0945 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

APN 806-2247
BR0901 MLB-MTG-BRKT-J5

POGO PINS

SH0950 SM — SHLD-J5-USB
SH0952 SM — SHLD-J5-CAN-FENCE-MDP-2
SH0951 SM — SHLD-J5-CAN-FENCE-MDP-1

SH0931 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0932 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0933 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0934 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0935 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0936 POGO-2.3OD-5.5H-SM-LOW-FORCE SM
SH0937 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0940 2.8OD1.2ID-1.35H-SM
SH0941 2.8OD1.2ID-1.35H-SM
SH0944 2.8OD1.2ID-1.35H-SM
SH0960 2.8OD1.2ID-1.35H-SM
SH0961 2.8OD1.2ID-1.35H-SM
SH0942 2.8OD1.2ID-1.35H-SM
SH0943 2.8OD1.2ID-1.35H-SM

T29 / GMUX JTAG Signals

TBT_LSOE<3> — TBT_LSEO_LSOE3 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<3>
TBT_LSOE<2> — TBT_LSEO_LSOE2 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TBT_LSEO<2>

GMUX ALIASES

82 EG_RESET_L (MAKE_BASE=TRUE) — GPU_RESET_L 71 78
18 LVDS_IG_BKL_ON (MAKE_BASE=TRUE) — IG_BKLT_EN 82
18 LVDS_IG_PANEL_PWR (MAKE_BASE=TRUE) — IG_LCD_PWR_EN 82
PEX_CLKREQ_L (MAKE_BASE=TRUE) — EG_CLKREQ_IN_L 78 82
17 PEG_CLKREQ_L (MAKE_BASE=TRUE) — EG_CLKREQ_OUT_L 82
82 DP_TBTSNK0_HPD_IG (MAKE_BASE=TRUE) — DPA_IG_HPD 18 82
82 DP_TBTSNK1_HPD_IG (MAKE_BASE=TRUE) — DPB_IG_HPD 18 82

17 PCIE_EXCARD_D2R_N — TRUE, MAKE_BASE=TRUE — NC_PCIE_EXCARD_D2R_N
17 PCIE_EXCARD_D2R_P — TRUE, MAKE_BASE=TRUE — NC_PCIE_EXCARD_D2R_P
17 PCIE_EXCARD_R2D_C_N — TRUE, MAKE_BASE=TRUE — NC_PCIE_EXCARD_R2D_C_N
17 PCIE_EXCARD_R2D_C_P — TRUE, MAKE_BASE=TRUE — NC_PCIE_EXCARD_R2D_C_P
92 17 PCIE_CLK100M_EXCARD_N — TRUE, MAKE_BASE=TRUE — NC_PCIE_CLK100M_EXCARD_N
92 17 PCIE_CLK100M_EXCARD_P — TRUE, MAKE_BASE=TRUE — NC_PCIE_CLK100M_EXCARD_P

17 TP_PCH_CLKOUT_DPN — TRUE, MAKE_BASE=TRUE — DPLL_REF_CLKN 11 89
17 TP_PCH_CLKOUT_DPP — TRUE, MAKE_BASE=TRUE — DPLL_REF_CLKP 11 89
17 TP_PCH_GPIO64_CLKOUTFLEX0 — TRUE, MAKE_BASE=TRUE — NC_PCH_GPIO64_CLKOUTFLEX0
17 TP_PCH_GPIO65_CLKOUTFLEX1 — TRUE, MAKE_BASE=TRUE — NC_PCH_GPIO65_CLKOUTFLEX1
17 TP_PCH_GPIO66_CLKOUTFLEX2 — TRUE, MAKE_BASE=TRUE — NC_PCH_GPIO66_CLKOUTFLEX2
17 TP_PCH_GPIO67_CLKOUTFLEX3 — TRUE, MAKE_BASE=TRUE — NC_PCH_GPIO67_CLKOUTFLEX3

SD_PWR_EN_PCH (MAKE_BASE=TRUE) — ENET_LOW_PWR_PCH 20 24 25
38 7 SD_PWR_EN (MAKE_BASE=TRUE) — ENET_LOW_PWR 25
TP_FW_PWR_EN (MAKE_BASE=TRUE) — FW_PWR_EN 25

SMT GND TEST PONTS

ZT0990 2.1SM2.0MM-CIR SMT-PAD-NSP
ZT0991 2.1SM2.0MM-CIR SMT-PAD-NSP
ZT0992 2.1SM2.0MM-CIR SMT-PAD-NSP
ZT0993 2.1SM2.0MM-CIR SMT-PAD-NSP

Digital Ground

MLB_RAMCFG0 — RAMCFG0:L R0910 1K 5% 1/20W MF 201
MLB_RAMCFG1 — RAMCFG1:L R0911 1K 5% 1/20W MF 201
MLB_RAMCFG2 — RAMCFG2:L R0912 1K 5% 1/20W MF 201
MLB_RAMCFG3 — RAMCFG3:L R0913 1K 5% 1/20W MF 201

CPU signals

CPU_VID<0..6> (MAKE_BASE=TRUE) — CPUIMVP_VID<0..6>
TP_CPU_VTT_SELECT (MAKE_BASE=TRUE) — CPU_VTTSELECT
27 MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN 27 64

Unused PEG signals

NC_PEG_D2R_P<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_D2R_P<15..14> 10
NC_PEG_D2R_N<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_D2R_N<15..14> 10
NC_PEG_R2D_C_P<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_R2D_C_P<15..14> 10
NC_PEG_R2D_C_N<15..14> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =PEG_R2D_C_N<15..14> 10

T29 Signals Through PEG

92 35 PCIE_TBT_D2R_P<3..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<11..8> 10
92 35 PCIE_TBT_D2R_N<3..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<11..8> 10
92 35 PCIE_TBT_R2D_C_P<3..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<11..8> 10
92 35 PCIE_TBT_R2D_C_N<3..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<11..8> 10

GPU signals

89 88 71 PEG_D2R_P<7..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<7..0> 10
89 88 71 PEG_D2R_N<7..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<7..0> 10
89 71 PEG_R2D_C_P<7..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<7..0> 10
89 71 PEG_R2D_C_N<7..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<7..0> 10

UNUSED TBT PORTS

TBT_D2R_P<3..2> — NC_TBT_D2RP<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_D2R_N<3..2> — NC_TBT_D2RN<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_R2D_C_P<3..2> — NC_TBT_R2D_CP<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)
TBT_R2D_C_N<3..2> — NC_TBT_R2D_CN<3..2> (MAKE_BASE=TRUE, NO_TEST=TRUE)

DPMUX TX & RX

82 DPMUX_UC_BOOT_TX (MAKE_BASE=TRUE) — DPMUX_UC_TX 82
82 DPMUX_UC_BOOT_RX (MAKE_BASE=TRUE) — DPMUX_UC_RX 82

SSD PCIE SIGNALS

92 39 PCIE_SSD_D2R_P<1..0> (MAKE_BASE=TRUE) — =PEG_D2R_P<13..12> 10
92 39 PCIE_SSD_D2R_N<1..0> (MAKE_BASE=TRUE) — =PEG_D2R_N<13..12> 10
92 39 PCIE_SSD_R2D_C_P<1..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_P<13..12> 10
92 39 PCIE_SSD_R2D_C_N<1..0> (MAKE_BASE=TRUE) — =PEG_R2D_C_N<13..12> 10
TP_PCIE_CLK100M_FW_P (MAKE_BASE=TRUE) — PCIE_CLK100M_FW_P 17 92
TP_PCIE_CLK100M_FW_N (MAKE_BASE=TRUE) — PCIE_CLK100M_FW_N 17 92

UNUSED FDI SIGNALS

NC_PCH_FDI_DATA_N<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_DATA_N<7..0> 18
NC_PCH_FDI_DATA_P<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_DATA_P<7..0> 18
NC_PCH_FDI_FSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_FSYNC<1..0> 18
NC_PCH_FDI_LSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — =FDI_LSYNC<1..0> 18
NC_CPU_FDI_DATA_N<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_DATA_N<7..0> 10 89
NC_CPU_FDI_DATA_P<7..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_DATA_P<7..0> 10 89
NC_CPU_FDI_FSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_FSYNC<1..0> 10 89
NC_CPU_FDI_LSYNC<1..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — FDI_LSYNC<1..0> 10 89

USB SIGNALS

91 34 USB_BT_P (MAKE_BASE=TRUE) — USBHUB_DN1_P 26
91 34 USB_BT_N (MAKE_BASE=TRUE) — USBHUB_DN1_N 26
91 49 USB_TPAD_P (MAKE_BASE=TRUE) — USBHUB_DN2_P 26
91 49 USB_TPAD_N (MAKE_BASE=TRUE) — USBHUB_DN2_N 26
91 41 USB_SMC_P (MAKE_BASE=TRUE) — USBHUB_DN3_P 26
91 41 USB_SMC_N (MAKE_BASE=TRUE) — USBHUB_DN3_N 26
PU_USBHUB_DN4P (MAKE_BASE=TRUE) — USBHUB_DN4_P 26
PU_USBHUB_DN4N (MAKE_BASE=TRUE) — USBHUB_DN4_N 26

8 =PP5V_S0_AUDIO_XW
XW0902 SM — PP5V_S0_AUDIO_AMP_L 57 (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V)
XW0903 SM — PP5V_S0_AUDIO_AMP_R 57 (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V)

LVDS_IG_A_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_P<3> 18 91
NC_LVDS_IG_A_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_N<3> 18 91
NC_LVDS_IG_B_DATAP<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_P<3> 18
NC_LVDS_IG_B_DATAN<3> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_N<3> 18
NC_LVDS_IG_A_CLK_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_CLK_N 18 91
NC_LVDS_IG_A_CLK_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_CLK_P 18 91
NC_LVDS_IG_A_DATA_N<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_N<2..0> 18 91
NC_LVDS_IG_A_DATA_P<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_A_DATA_P<2..0> 18 91
NC_LVDS_IG_B_DATA_N<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_N<2..0> 18 91
NC_LVDS_IG_B_DATA_P<2..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_B_DATA_P<2..0> 18 91
NC_LVDS_IG_DDC_CLK (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_DDC_CLK 18
NC_LVDS_IG_DDC_DATA (MAKE_BASE=TRUE, NO_TEST=TRUE) — LVDS_IG_DDC_DATA 18
NC_PCIE_FW_D2RN (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_D2R_N 17
NC_PCIE_FW_D2RP (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_D2R_P 17
NC_PCIE_FW_R2D_CN (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_R2D_C_N 17
NC_PCIE_FW_R2D_CP (MAKE_BASE=TRUE, NO_TEST=TRUE) — PCIE_FW_R2D_C_P 17
NC_SATA_ODD_D2R_N (MAKE_BASE=TRUE) — SATA_ODD_D2R_N 17 91
NC_SATA_ODD_D2R_P (MAKE_BASE=TRUE) — SATA_ODD_D2R_P 17 91
NC_SATA_ODD_R2D_C_N (MAKE_BASE=TRUE) — SATA_ODD_R2D_C_N 17 91
NC_SATA_ODD_R2D_C_P (MAKE_BASE=TRUE) — SATA_ODD_R2D_C_P 17 91
NC_DP_IG_MLP<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_DP_IG_B_MLP<3..0> 18
NC_DP_IG_MLN<3..0> (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_DP_IG_B_MLN<3..0> 18

TBTBST:N
37 8 =PPVIN_SW_TBTBST — R0950 0 5% 1/8W MF-LF 805 — =PP15V_TBT_REG 8 37

UNUSED USB SIGNALS

NC_USB3_EXTD_TX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_TX_P 19
NC_USB3_EXTD_TX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_TX_N 19
NC_USB3_EXTD_RX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_RX_P 19
NC_USB3_EXTD_RX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTD_RX_N 19
NC_USB_EXTD_EHCI_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTD_EHCI_P 19
NC_USB_EXTD_EHCI_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTD_EHCI_N 19
NC_USB3_EXTC_TX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_TX_P 19 91
NC_USB3_EXTC_TX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_TX_N 19 91
NC_USB3_EXTC_RX_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_RX_P 19 91
NC_USB3_EXTC_RX_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB3_EXTC_RX_N 19 91
NC_USB_EXTC_P (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTC_P 19 91
NC_USB_EXTC_N (MAKE_BASE=TRUE, NO_TEST=TRUE) — USB_EXTC_N 19 91

SYNC MASTER=D2 KEPLER — SYNC DATE=01/13/2012
PAGE TITLE: Signal Aliases

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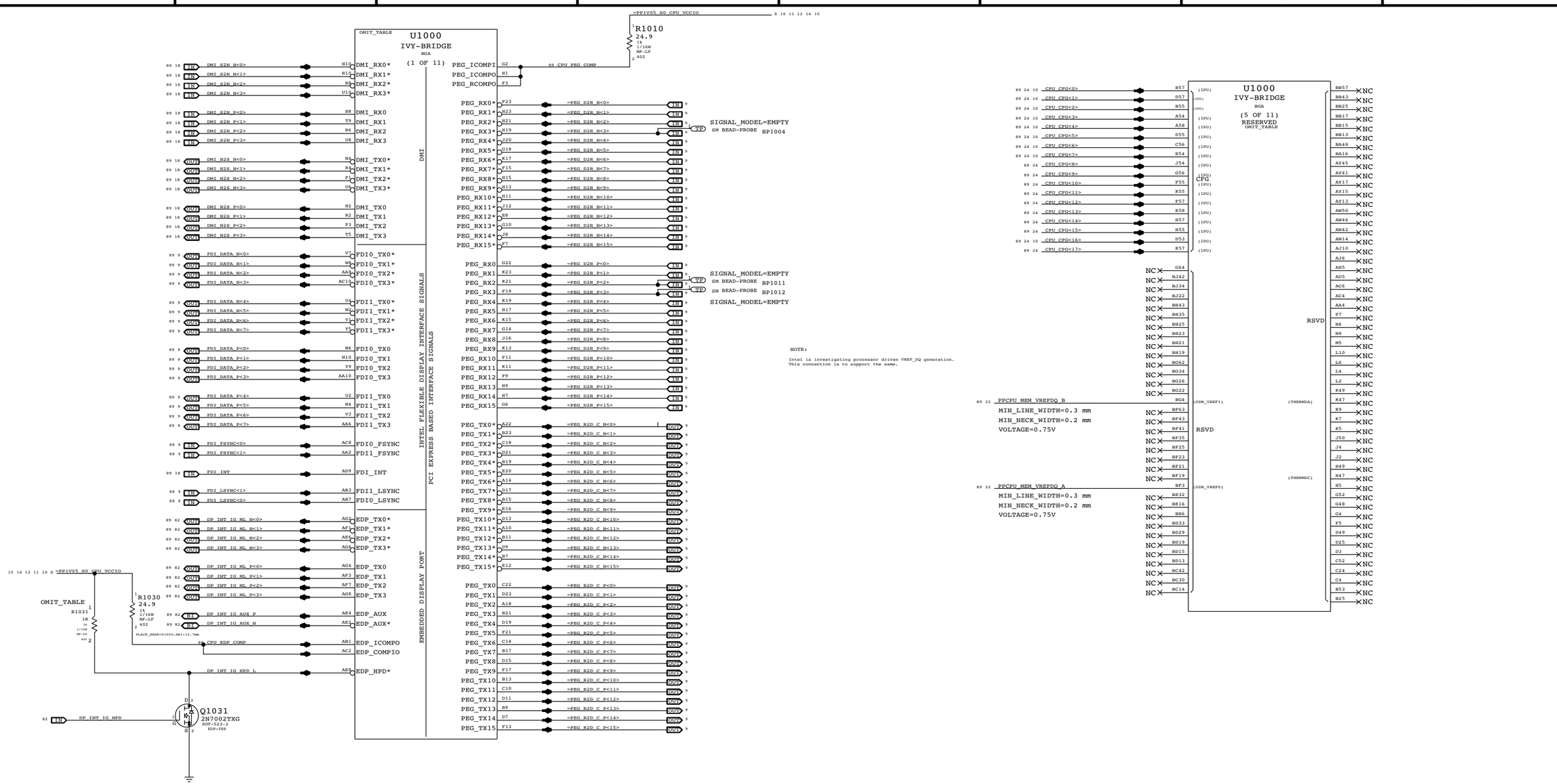

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1%,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10%,0402,SMD,LF	R1031		EDP:NO

CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

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CPU DMI/PEG/FDI/RSVD

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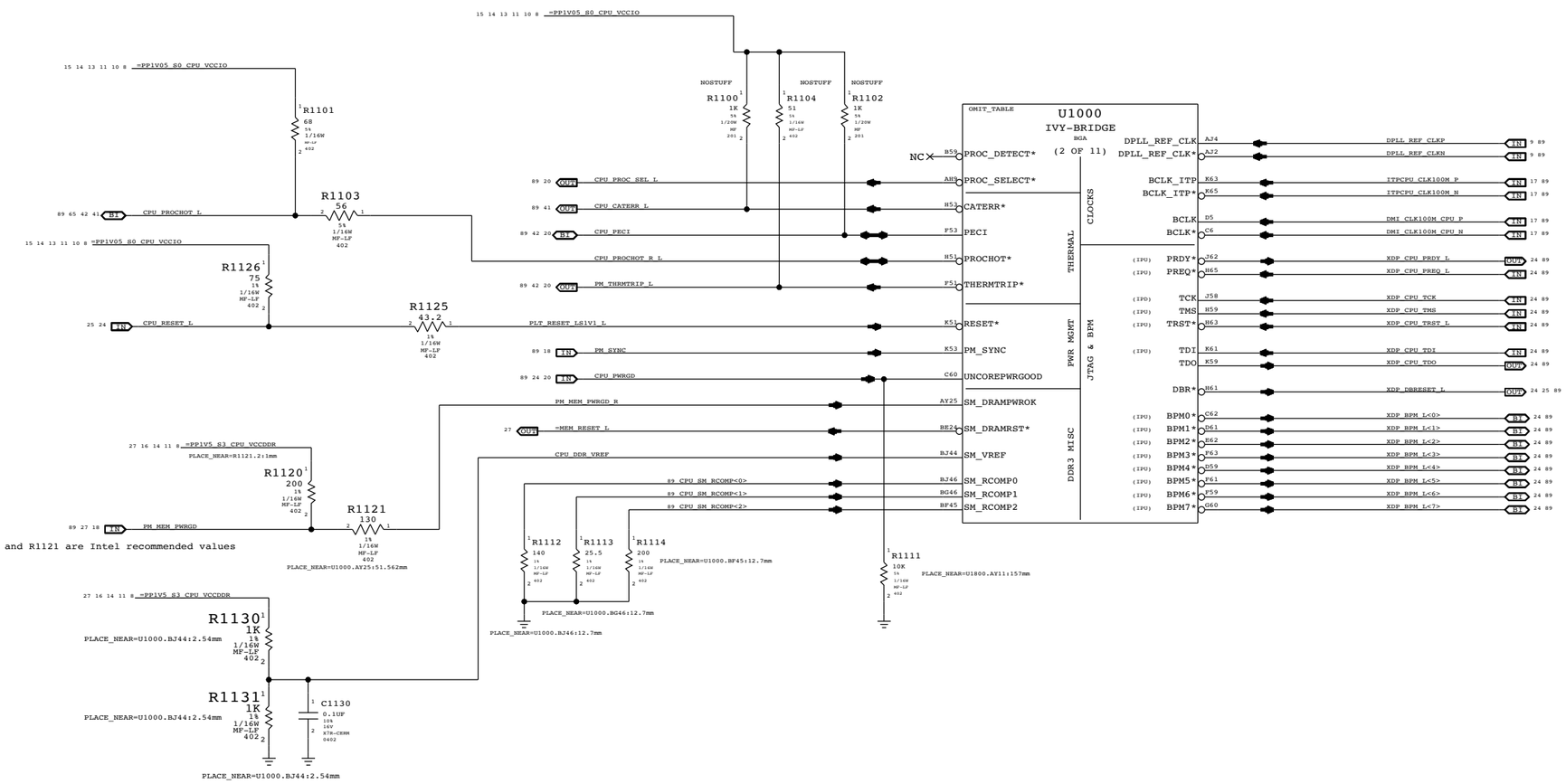

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CPU CLOCK/MISC/JTAG

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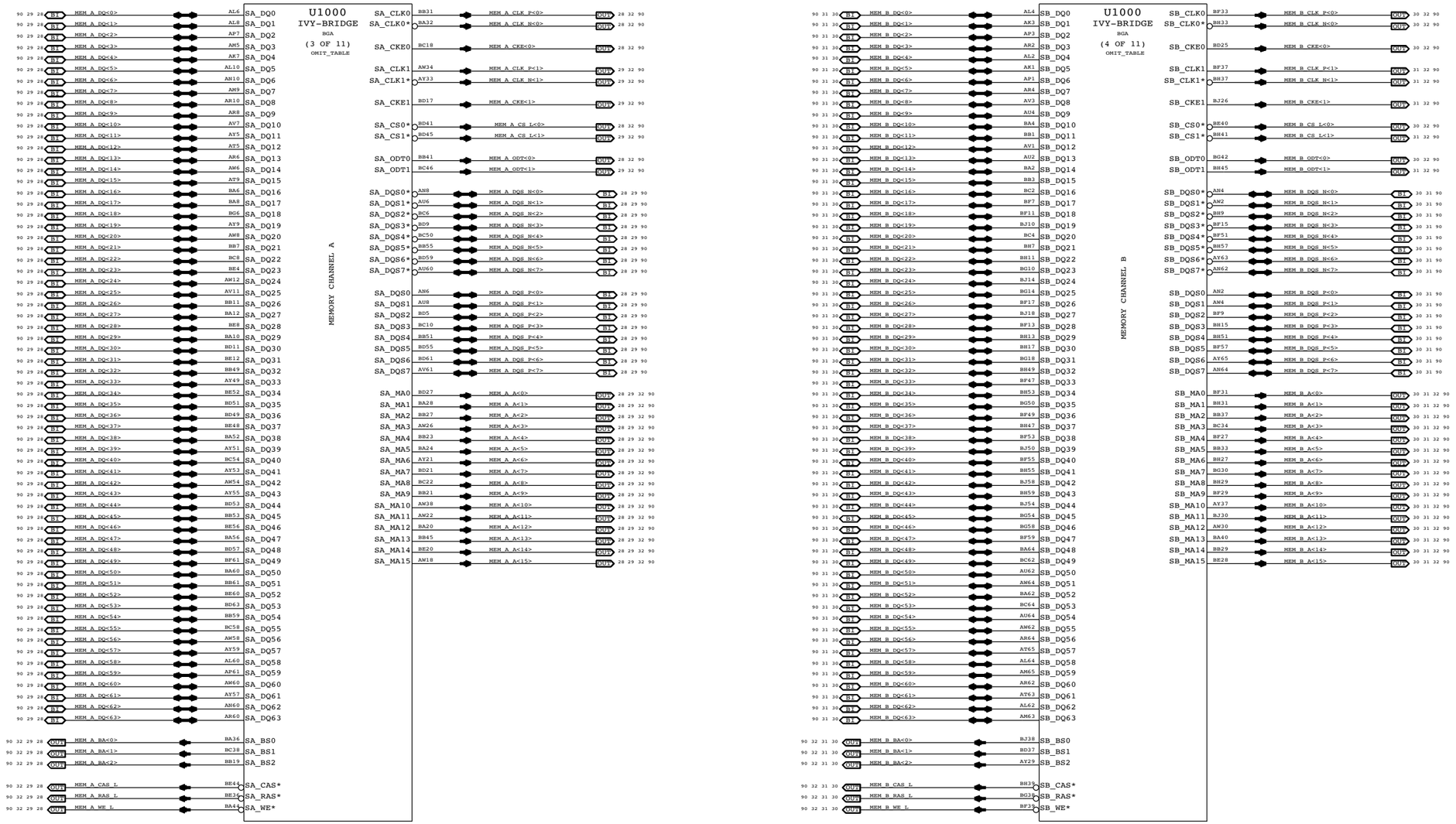

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CPU DDR3 INTERFACES

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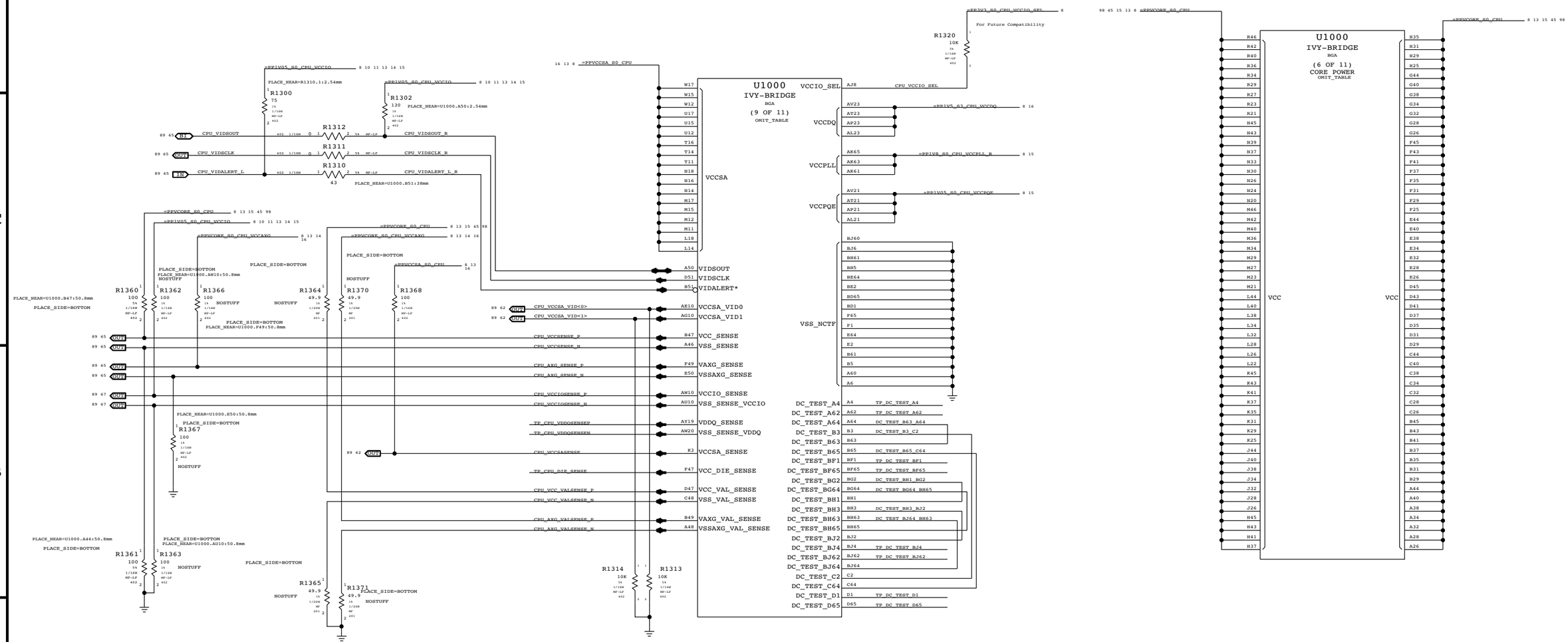

NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

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CPU POWER

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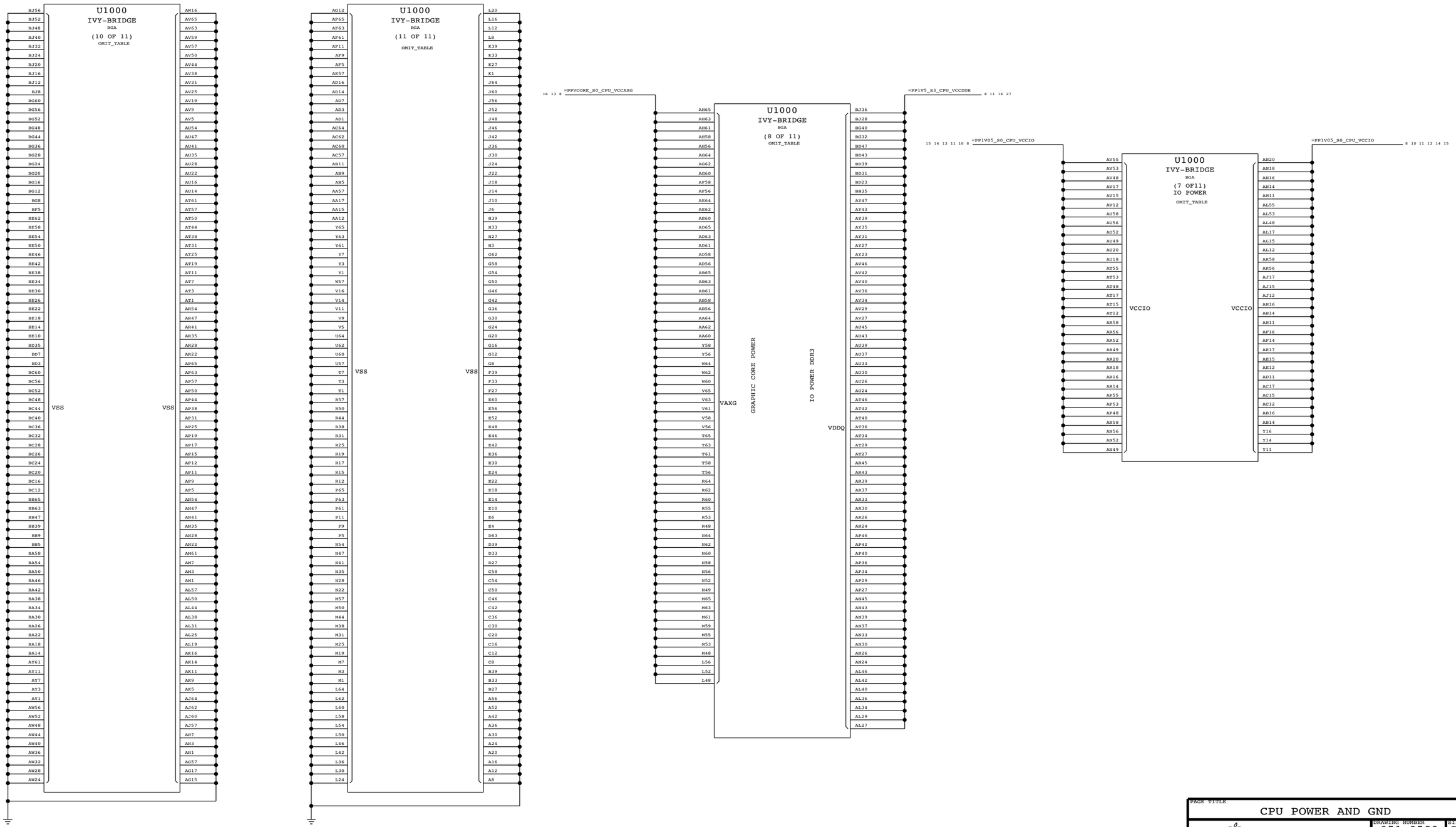

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CPU POWER AND GND

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm , 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

98 45 13 8 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X6S-CERM 0402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 4V CERM-X6S 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 4V CERM-X6S 0201

PLACEMENT_NOTE (C1620-C1623):
Place near inductors on bottom side.
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 4V X6S 0402

NOSTUFF CRITICAL C1690 C1691 C1698 C1693 C1694 C1695 C1696 C1699
20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
20UF 20% 2V X6T-CERM 0402

NOSTUFF C16D0 C16D1 C16D2 C16D3 C16D4 C16D5
20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):

CRITICAL C1640 C1641 C1642 C1643 C1644 C1645 C1688 C1689
270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 11 10 8 14 =PP1V05_S0_CPU_VCCIO

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X6S-CERM 0402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 4V X6S-CERM 0603

CRITICAL C1682 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1683 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 =PP1V05_S0_CPU_VCCPQE 8 13
C1684 1UF 10% 10V X6S-CERM 0402

CPU VCCPLL DECOUPLING

8 =PP1V8_S0_CPU_VCCPLL R1600 0 5% 1/16W MF-LF 402 =PP1V8_S0_CPU_VCCPLL_R 8 13
C1685 1UF 10% 10V X6S-CERM 0402
C1686 1UF 10% 10V X6S-CERM 0402
PLACE_NEAR=U1000.AK61:5MM
CRITICAL C1687 220UF 20% 2.5V TANT B16 (Z = 1.2mm, place on short side behind CPU)
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC MASTER=D2 SEAN SYNC DATE=03/05/2012

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VAXG DECOUPLING

INTEL RECOMMENDATION: 2X 470UF 4MOHM, 2X 470UF 4MOHM (NOSTUFF), 6X 22UF 0805, 2X 22UF 0805 (NOSTUFF), 6X 10UF 0603, 2X 10UF 0603 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)
APPLE IMPLEMENTATION: 0X 470UF 4MOHM, 3X 330UF 9MOHM , 6X 22UF 0603, 2X 22UF 0603 (NOSTUFF), 6X 10UF 0402, 2X 10UF 0402 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)

14 13 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X6S-CERM 0402
C1701 1UF 10% 10V X6S-CERM 0402
C1702 1UF 10% 10V X6S-CERM 0402
C1703 1UF 10% 10V X6S-CERM 0402
C1704 1UF 10% 10V X6S-CERM 0402
C1705 1UF 10% 10V X6S-CERM 0402
C1706 1UF 10% 10V X6S-CERM 0402
C1707 1UF 10% 10V X6S-CERM 0402
C1708 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1709 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1710 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1711 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1712 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1713 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1714 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1715 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1716 1UF 10% 10V X6S-CERM 0402
NOSTUFF C1717 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 4V X6S 0402
C1719 10UF 20% 4V X6S 0402
C1720 10UF 20% 4V X6S 0402
C1721 10UF 20% 4V X6S 0402
C1722 10UF 20% 4V X6S 0402
C1723 10UF 20% 4V X6S 0402
NOSTUFF C1724 10UF 20% 4V X6S 0402
NOSTUFF C1725 10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 4V X6S 0603
C1727 22UF 20% 4V X6S 0603
C1728 22UF 20% 4V X6S 0603
C1729 22UF 20% 4V X6S 0603
C1730 22UF 20% 4V X6S 0603
C1731 22UF 20% 4V X6S 0603
NOSTUFF C1732 22UF 20% 4V X6S 0603
NOSTUFF C1733 22UF 20% 4V X6S 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1735 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1737 330UF-6MOHM 20% 2.0V POLY-TANT D15T

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

27 14 11 8 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 1UF 10% 10V X6S-CERM 0402
C1739 1UF 10% 10V X6S-CERM 0402
C1740 1UF 10% 10V X6S-CERM 0402
C1741 1UF 10% 10V X6S-CERM 0402
C1742 1UF 10% 10V X6S-CERM 0402
C1743 1UF 10% 10V X6S-CERM 0402
C1744 1UF 10% 10V X6S-CERM 0402
C1745 1UF 10% 10V X6S-CERM 0402
C1746 1UF 10% 10V X6S-CERM 0402
C1747 1UF 10% 10V X6S-CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 4V X6S-CERM 0603
C1749 10UF 20% 4V X6S-CERM 0603
C1750 10UF 20% 4V X6S-CERM 0603
C1751 10UF 20% 4V X6S-CERM 0603
C1752 10UF 20% 4V X6S-CERM 0603
C1753 10UF 20% 4V X6S-CERM 0603
C1754 10UF 20% 4V X6S-CERM 0603
C1755 10UF 20% 4V X6S-CERM 0603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603
=PP1V5_S3_PHL_VCCDQ 8 13
C1757 1UF 10% 10V X6S-CERM 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 1UF 10% 10V X6S-CERM 0402
C1759 1UF 10% 10V X6S-CERM 0402
C1760 1UF 10% 10V X6S-CERM 0402
C1761 1UF 10% 10V X6S-CERM 0402
C1762 1UF 10% 10V X6S-CERM 0402

C1763 10UF 20% 4V X6S-CERM 0603
C1764 10UF 20% 4V X6S-CERM 0603
C1765 10UF 20% 4V X6S-CERM 0603
C1766 10UF 20% 4V X6S-CERM 0603
C1767 10UF 20% 4V X6S-CERM 0603

CRITICAL C1768 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

SYNC MASTER=D2 SEAN SYNC DATE=03/05/2012

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

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BRANCH:
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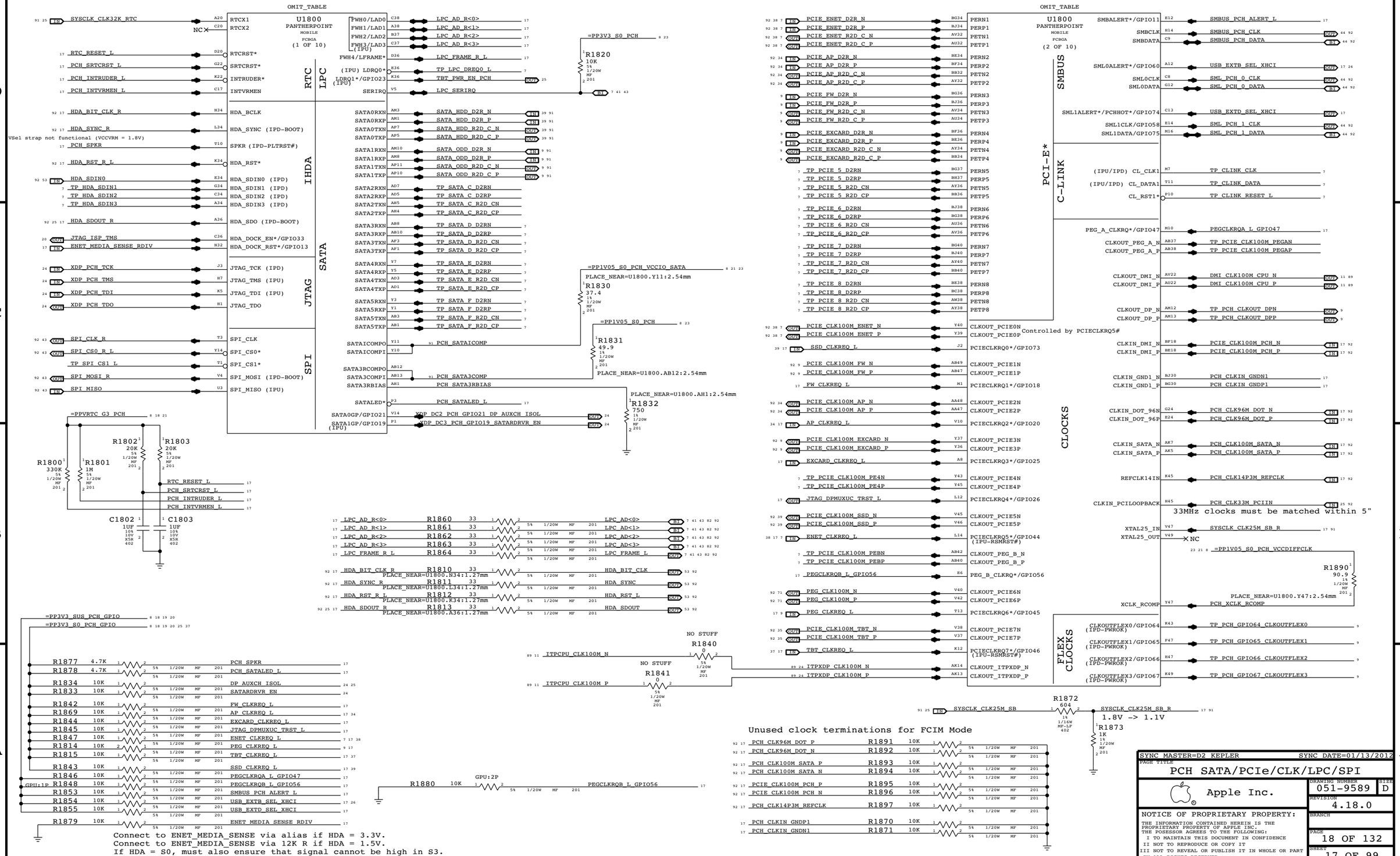
OMIT_TABLE
U1800
PANTHERPOINT
MOBILE
FCBGA
(1 OF 10)
(2 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SMBUS
C-LINK
PCI-E*
CLOCKS
FLEX CLOCKS
SYSCLK_CLK32K_RTC
NC
RTCX1
RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
VSel strap not functional (VCCVRM = 1.8V)
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
=PPVRTC_G3_PCH
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
=PP3V3_S0_PCH
R1820 10K
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4
=PP1V05_S0_PCH
R1831 49.9
PLACE_NEAR=U1800.AB12:2.54mm
PLACE_NEAR=U1800.AH1:2.54mm
R1832 750
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1877 4.7K
R1878 4.7K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
NO STUFF
R1840 0
R1841 0
R1880 10K
GPU:2P
R1872 604
R1873 1K
1.8V -> 1.1V
Controlled by PCIECLKRQ5#
33MHz clocks must be matched within 5"
Unused clock terminations for FCIM Mode
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1870 10K
R1871 10K
SYNC MASTER=D2 KEPLER
SYNC DATE=01/13/2012
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
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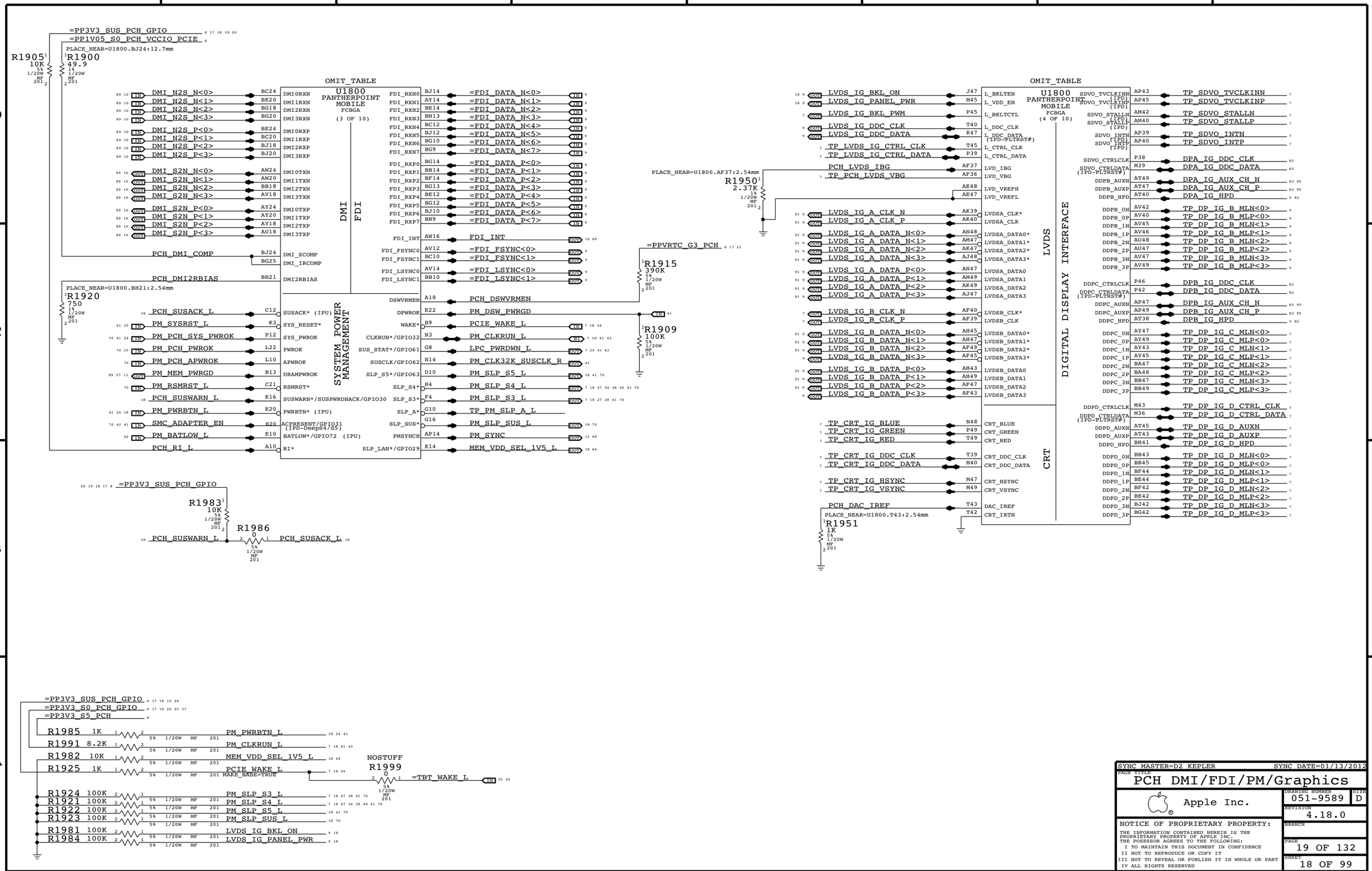
U1800
PANTHERPOINT MOBILE
FCBGA
(3 OF 10)
DMI
FDI
SYSTEM POWER MANAGEMENT
U1800
PANTHERPOINT MOBILE
FCBGA
(4 OF 10)
LVDS
DIGITAL DISPLAY INTERFACE
CRT
OMIT_TABLE
=PP3V3_SUS_PCH_GPIO
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.BJ24:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI_COMP
PCH_DMI2RBIAS
PLACE_NEAR=U1800.BH21:2.54mm
R1920 750 1% 1/20W MF 201
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_APWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
=FDI_DATA_N<0>
=FDI_DATA_N<1>
=FDI_DATA_N<2>
=FDI_DATA_N<3>
=FDI_DATA_N<4>
=FDI_DATA_N<5>
=FDI_DATA_N<6>
=FDI_DATA_N<7>
=FDI_DATA_P<0>
=FDI_DATA_P<1>
=FDI_DATA_P<2>
=FDI_DATA_P<3>
=FDI_DATA_P<4>
=FDI_DATA_P<5>
=FDI_DATA_P<6>
=FDI_DATA_P<7>
FDI_INT
=FDI_FSYNC<0>
=FDI_FSYNC<1>
=FDI_LSYNC<0>
=FDI_LSYNC<1>
=PPVRTC_G3_PCH
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
MEM_VDD_SEL_1V5_L
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
LVDS_IG_BKL_PWM
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
TP_LVDS_IG_CTRL_CLK
TP_LVDS_IG_CTRL_DATA
PCH_LVDS_IBG
TP_PCH_LVDS_VBG
PLACE_NEAR=U1800.AF37:2.54mm
R1950 2.37K 1% 1/20W MF 201
LVDS_IG_A_CLK_N
LVDS_IG_A_CLK_P
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_N<3>
LVDS_IG_A_DATA_P<0>
LVDS_IG_A_DATA_P<1>
LVDS_IG_A_DATA_P<2>
LVDS_IG_A_DATA_P<3>
LVDS_IG_B_CLK_N
LVDS_IG_B_CLK_P
LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_N<2>
LVDS_IG_B_DATA_N<3>
LVDS_IG_B_DATA_P<0>
LVDS_IG_B_DATA_P<1>
LVDS_IG_B_DATA_P<2>
LVDS_IG_B_DATA_P<3>
TP_CRT_IG_BLUE
TP_CRT_IG_GREEN
TP_CRT_IG_RED
TP_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA
TP_CRT_IG_HSYNC
TP_CRT_IG_VSYNC
PCH_DAC_IREF
PLACE_NEAR=U1800.T43:2.54mm
R1951 1K 5% 1/20W MF 201
TP_SDVO_TVCLKINN
TP_SDVO_TVCLKINP
TP_SDVO_STALLN
TP_SDVO_STALLP
TP_SDVO_INTN
TP_SDVO_INTP
DPA_IG_DDC_CLK
DPA_IG_DDC_DATA
DPA_IG_AUX_CH_N
DPA_IG_AUX_CH_P
DPA_IG_HPD
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA
DPB_IG_AUX_CH_N
DPB_IG_AUX_CH_P
DPB_IG_HPD
TP_DP_IG_B_MLN<0>
TP_DP_IG_B_MLP<0>
TP_DP_IG_B_MLN<1>
TP_DP_IG_B_MLP<1>
TP_DP_IG_B_MLN<2>
TP_DP_IG_B_MLP<2>
TP_DP_IG_B_MLN<3>
TP_DP_IG_B_MLP<3>
TP_DP_IG_C_MLN<0>
TP_DP_IG_C_MLP<0>
TP_DP_IG_C_MLN<1>
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TP_DP_IG_C_MLP<2>
TP_DP_IG_C_MLN<3>
TP_DP_IG_C_MLP<3>
TP_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA
TP_DP_IG_D_AUXN
TP_DP_IG_D_AUXP
TP_DP_IG_D_HPD
TP_DP_IG_D_MLN<0>
TP_DP_IG_D_MLP<0>
TP_DP_IG_D_MLN<1>
TP_DP_IG_D_MLP<1>
TP_DP_IG_D_MLN<2>
TP_DP_IG_D_MLP<2>
TP_DP_IG_D_MLN<3>
TP_DP_IG_D_MLP<3>
=PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
PCH_SUSWARN_L
PCH_SUSACK_L
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
=PP3V3_S5_PCH
R1985 1K
R1991 8.2K
R1982 10K
R1925 1K
PM_PWRBTN_L
PM_CLKRUN_L
MEM_VDD_SEL_1V5_L
PCIE_WAKE_L
MAKE_BASE=TRUE
NOSTUFF
R1999 0 5% 1/20W MF 201
=TBT_WAKE_L
R1924 100K
R1921 100K
R1922 100K
R1923 100K
R1981 100K
R1984 100K
PM_SLP_S3_L
PM_SLP_S4_L
PM_SLP_S5_L
PM_SLP_SUS_L
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
SYNC MASTER=D2_KEPLER
SYNC DATE=01/13/2012
PAGE TITLE
PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
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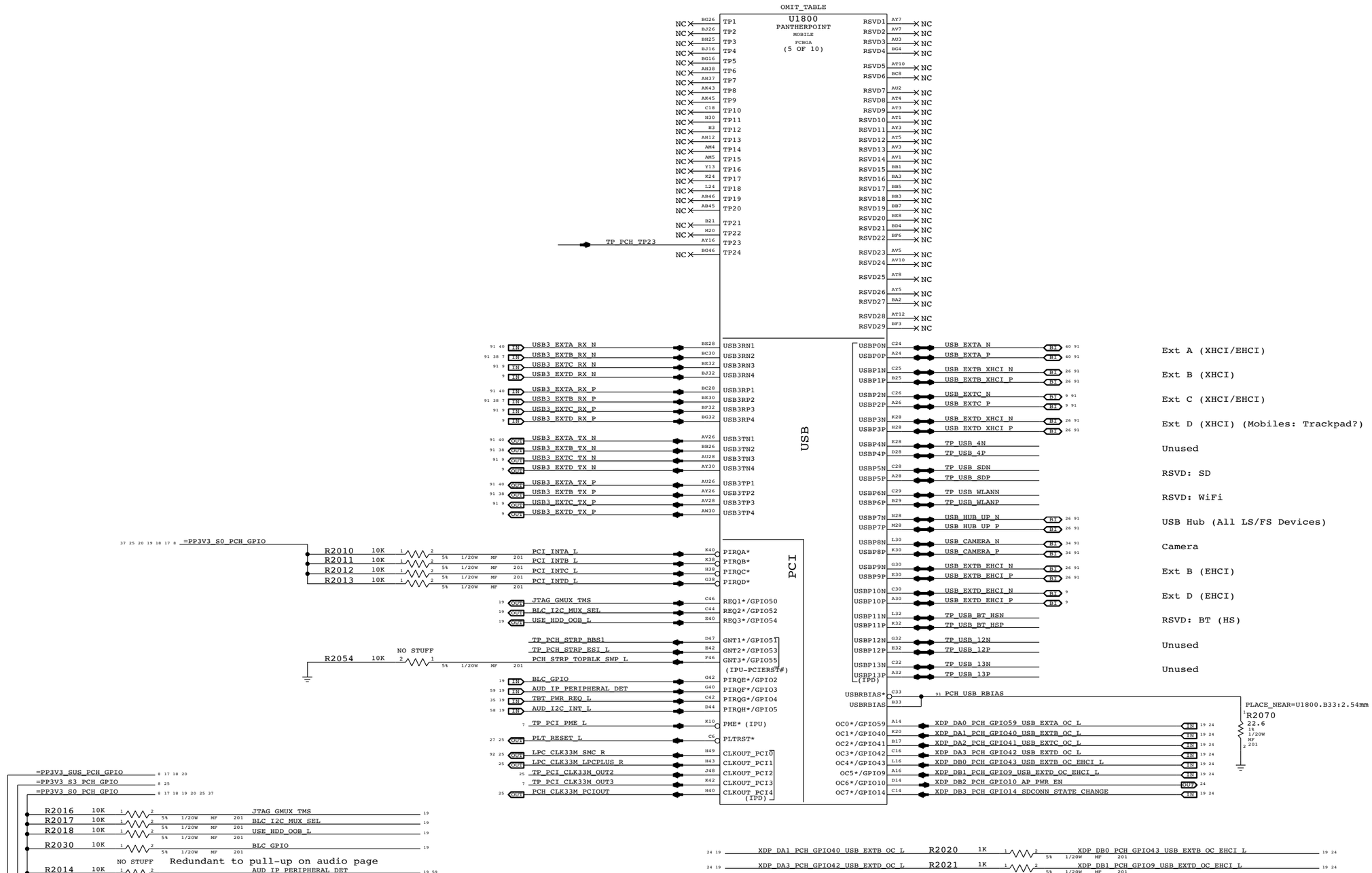

SYNC MASTER=D2 KEPLER	SYNC DATE=01/13/2012
PAGE TITLE: PCH PCI/USB/TP/RSVD	
Apple Inc.	DRAWING NUMBER: 051-9589 SIZE: D
	REVISION: 4.18.0
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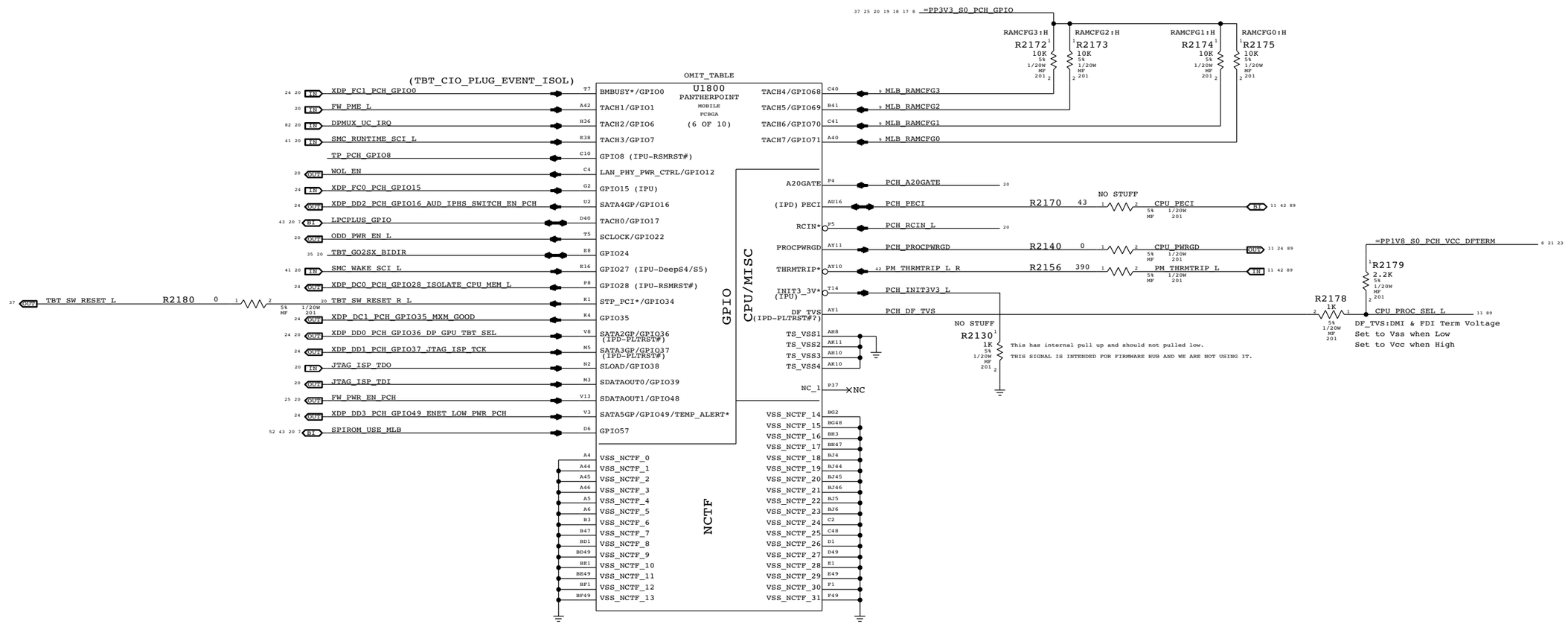
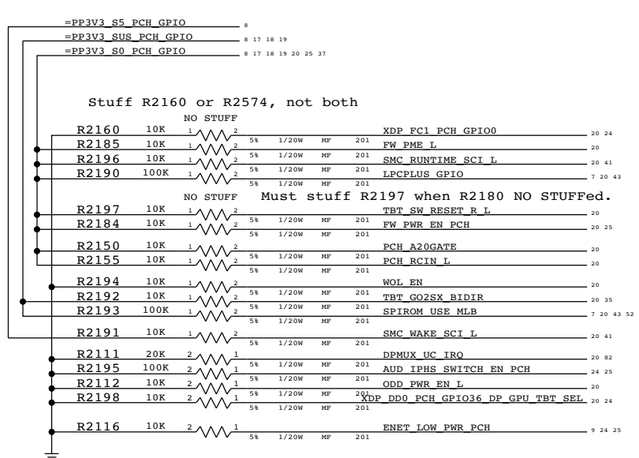
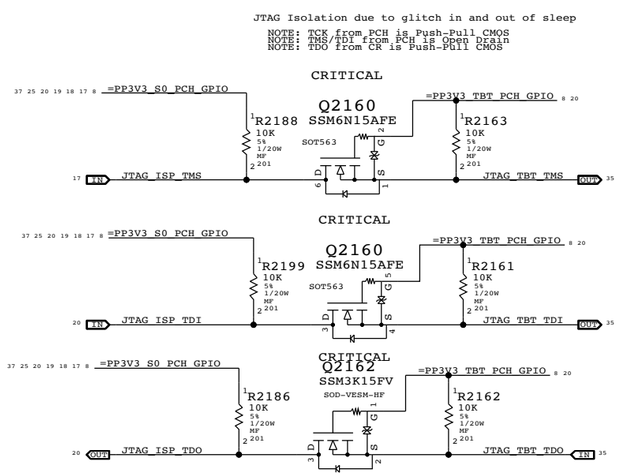
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

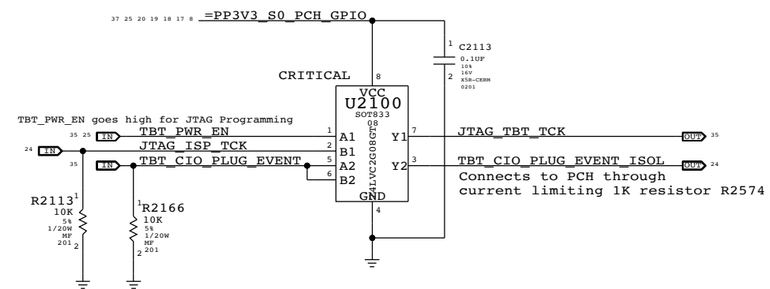
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.









SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

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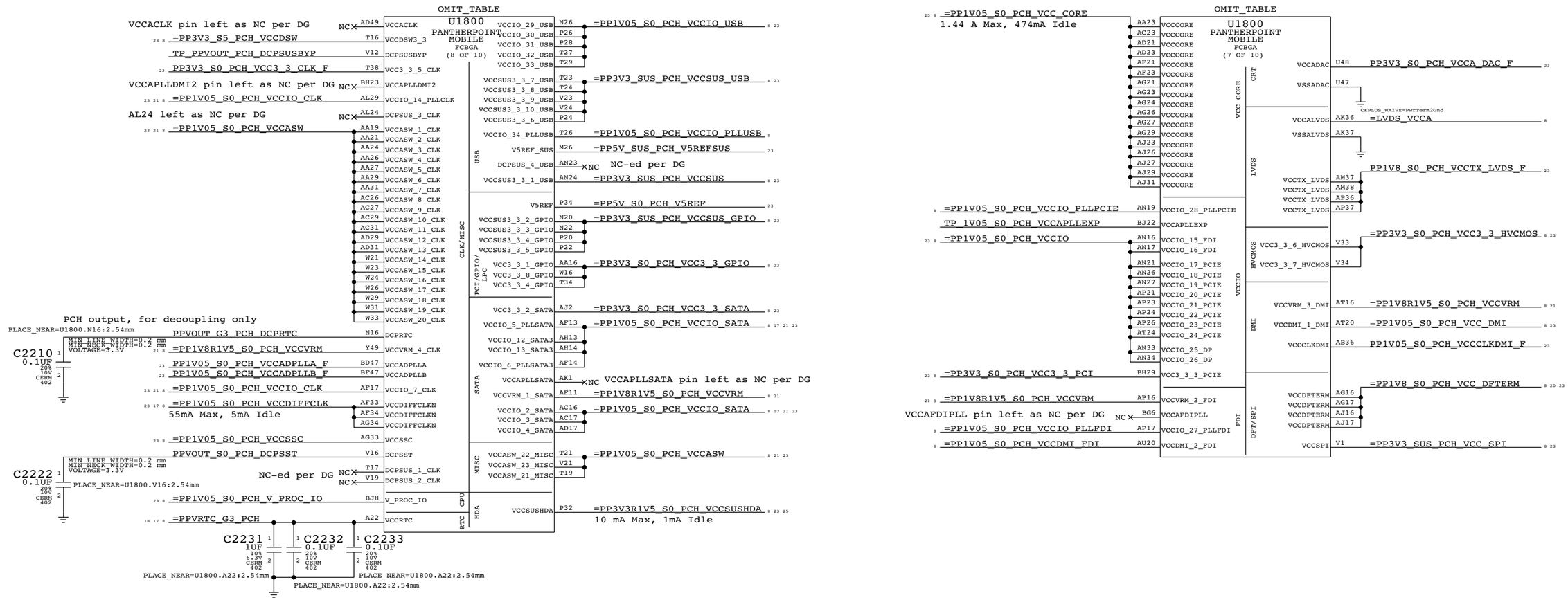

SYNC MASTER=D2 CLEAN SYNC DATE=03/19/2012

PAGE TITLE

PCH POWER

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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(9 OF 10)
VSS

H5	VSS	VSS	AK38
AA17	VSS	VSS	AK4
AA2	VSS	VSS	AK42
AA3	VSS	VSS	AK46
AA33	VSS	VSS	AK8
AA34	VSS	VSS	AL16
AB11	VSS	VSS	AL17
AB14	VSS	VSS	AL19
AB39	VSS	VSS	AL2
AB4	VSS	VSS	AL21
AB43	VSS	VSS	AL23
AB5	VSS	VSS	AL26
AB7	VSS	VSS	AL27
AC19	VSS	VSS	AL31
AC2	VSS	VSS	AL33
AC21	VSS	VSS	AL34
AC24	VSS	VSS	AL48
AC33	VSS	VSS	AM11
AC34	VSS	VSS	AM14
AC48	VSS	VSS	AM36
AD10	VSS	VSS	AM39
AD11	VSS	VSS	AM43
AD12	VSS	VSS	AM45
AD13	VSS	VSS	AM46
AD19	VSS	VSS	AM7
AD24	VSS	VSS	AN2
AD26	VSS	VSS	AN29
AD27	VSS	VSS	AN3
AD33	VSS	VSS	AN31
AD34	VSS	VSS	AP12
AD36	VSS	VSS	AP19
AD37	VSS	VSS	AP28
AD38	VSS	VSS	AP30
AD39	VSS	VSS	AP32
AD4	VSS	VSS	AP38
AD40	VSS	VSS	AP4
AD42	VSS	VSS	AP42
AD43	VSS	VSS	AP46
AD45	VSS	VSS	AP8
AD46	VSS	VSS	AR2
AD8	VSS	VSS	AR48
AE2	VSS	VSS	AT11
AE3	VSS	VSS	AT13
AF10	VSS	VSS	AT18
AF12	VSS	VSS	AT22
AD14	VSS	VSS	AT26
AD16	VSS	VSS	AT28
AF16	VSS	VSS	AT30
AF19	VSS	VSS	AT32
AF24	VSS	VSS	AT34
AF26	VSS	VSS	AT39
AF27	VSS	VSS	AT42
AF29	VSS	VSS	AT46
AF31	VSS	VSS	AT7
AF38	VSS	VSS	AU24
AF4	VSS	VSS	AU30
AF42	VSS	VSS	AV11
AF46	VSS	VSS	AV16
AF5	VSS	VSS	AV20
AF7	VSS	VSS	AV24
AF8	VSS	VSS	AV30
AG19	VSS	VSS	AV38
AG2	VSS	VSS	AV4
AG31	VSS	VSS	AV43
AG48	VSS	VSS	AV8
AH11	VSS	VSS	AW14
AH3	VSS	VSS	AW18
AH36	VSS	VSS	AW2
AH39	VSS	VSS	AW22
AH40	VSS	VSS	AW26
AH42	VSS	VSS	AW28
AH46	VSS	VSS	AW32
AH7	VSS	VSS	AW34
AJ19	VSS	VSS	AW36
AJ21	VSS	VSS	AW40
AJ24	VSS	VSS	AW48
AJ33	VSS	VSS	AY12
AJ34	VSS	VSS	AY22
AK12	VSS	VSS	AY28
AK3	VSS		

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(10 OF 10)
VSS

AY4	VSS	VSS	H46
AY42	VSS	VSS	K18
AY46	VSS	VSS	K26
AY8	VSS	VSS	K39
B11	VSS	VSS	K46
B15	VSS	VSS	K7
B19	VSS	VSS	L18
B23	VSS	VSS	L2
B27	VSS	VSS	L20
B31	VSS	VSS	L26
B35	VSS	VSS	L28
B39	VSS	VSS	L36
B7	VSS	VSS	L48
F45	VSS	VSS	M12
BB12	VSS	VSS	P16
BB16	VSS	VSS	M18
BB20	VSS	VSS	M22
BB22	VSS	VSS	M24
BB24	VSS	VSS	M30
BB28	VSS	VSS	M32
BB30	VSS	VSS	M34
BB38	VSS	VSS	M38
BB4	VSS	VSS	M4
BB46	VSS	VSS	M42
BC14	VSS	VSS	M46
BC18	VSS	VSS	M8
BC2	VSS	VSS	N18
BC22	VSS	VSS	P30
BC26	VSS	VSS	N47
BC32	VSS	VSS	P11
BC34	VSS	VSS	P18
BC36	VSS	VSS	T33
BC40	VSS	VSS	P40
BC42	VSS	VSS	P43
BC48	VSS	VSS	P47
BD46	VSS	VSS	P7
BD5	VSS	VSS	R2
BE22	VSS	VSS	R48
BE26	VSS	VSS	T12
BE40	VSS	VSS	T31
BF10	VSS	VSS	T37
BF12	VSS	VSS	T4
BF16	VSS	VSS	W34
BF20	VSS	VSS	T46
BF22	VSS	VSS	T47
BF24	VSS	VSS	T8
BF26	VSS	VSS	V11
BF28	VSS	VSS	V17
BD3	VSS	VSS	V26
BF30	VSS	VSS	V27
BF38	VSS	VSS	V29
BF40	VSS	VSS	V31
BF8	VSS	VSS	V36
BG17	VSS	VSS	V39
BG21	VSS	VSS	V43
BG33	VSS	VSS	V7
BG44	VSS	VSS	W17
BG8	VSS	VSS	W19
BH11	VSS	VSS	W2
BH15	VSS	VSS	W27
BH17	VSS	VSS	W48
BH19	VSS	VSS	Y12
H10	VSS	VSS	Y38
BH27	VSS	VSS	Y4
BH31	VSS	VSS	Y42
BH33	VSS	VSS	Y46
BH35	VSS	VSS	Y8
BH39	VSS		
BH43	VSS		
BH7	VSS	VSS	BG29
D3	VSS	VSS	N24
D12	VSS	VSS	AJ3
D16	VSS	VSS	AD47
D18	VSS		
D22	VSS	VSS	B43
D24	VSS	VSS	BE10
D26	VSS	VSS	BG41
D30	VSS		
D32	VSS	VSS	G14
D34	VSS	VSS	H16
D38	VSS		
D42	VSS	VSS	T36
D8	VSS		
E18	VSS	VSS	BG22
E26	VSS	VSS	BG24
G18	VSS	VSS	C22
G20	VSS	VSS	AP13
G26	VSS	VSS	M14
G28	VSS	VSS	AP3
G36	VSS	VSS	AP1
G48	VSS	VSS	BE16
H12	VSS	VSS	BC16
H18	VSS	VSS	BG28
H22	VSS	VSS	BJ28
H24	VSS		
H26	VSS		
H30	VSS		
H32	VSS		
H34	VSS		
F3	VSS		

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
PCH GROUNDS

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DRAWING NUMBER 051-9589 SIZE D

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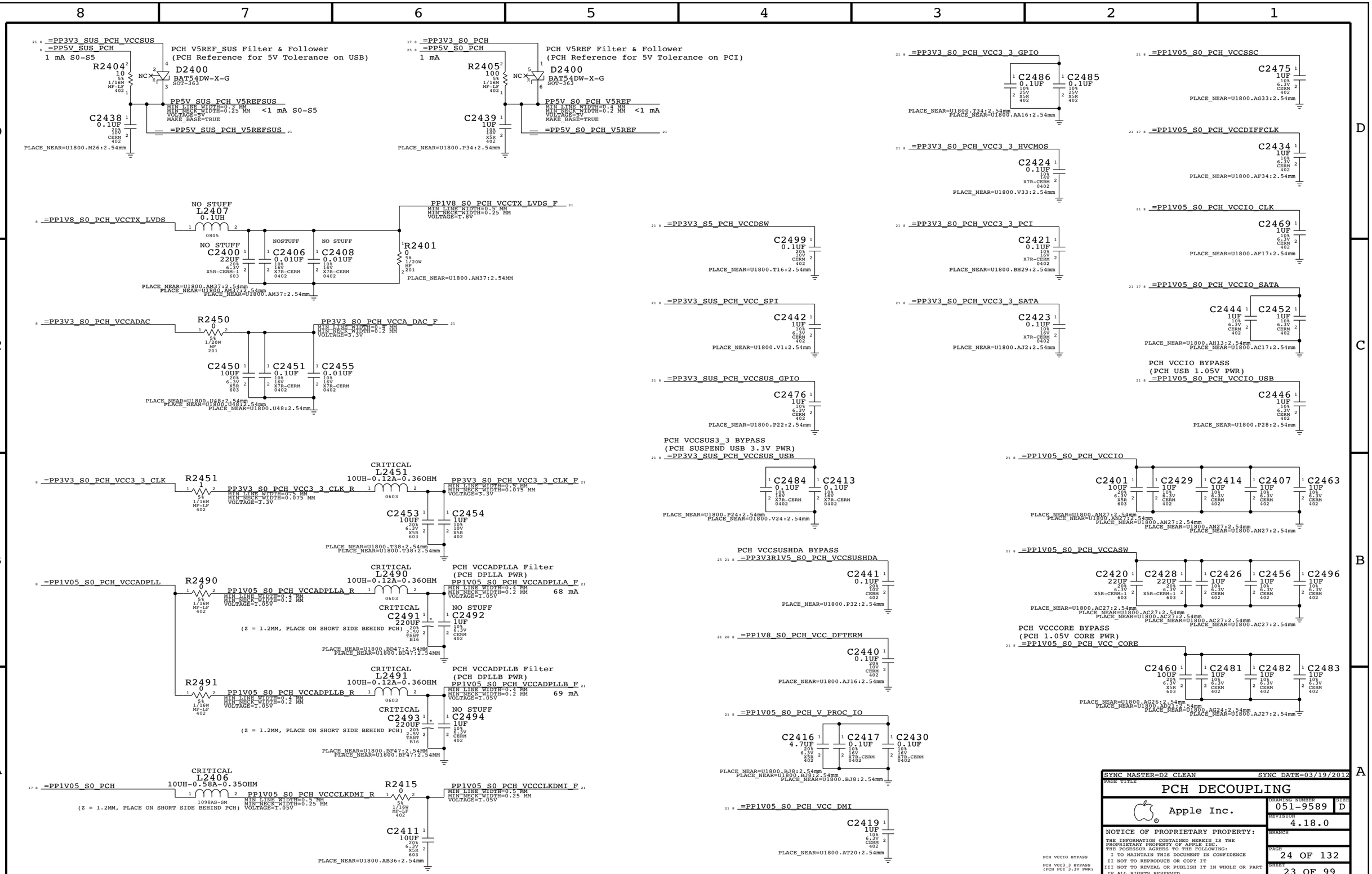
PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)
=PP3V3_SUS_PCH_VCCSUS
=PP5V_SUS_PCH
1 mA S0-S5
R2404 10 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_SUS_PCH_V5REFSUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 mA S0-S5
C2438 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.M26:2.54mm
=PP5V_SUS_PCH_V5REFSUS
PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)
=PP3V3_S0_PCH
=PP5V_S0_PCH
1 mA
R2405 100 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 mA
C2439 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.P34:2.54mm
=PP5V_S0_PCH_V5REF
=PP3V3_S0_PCH_VCC3_3_GPIO
C2486 0.1UF 10% 25V X5R 402
C2485 0.1UF 10% 25V X5R 402
PLACE_NEAR=U1800.T34:2.54mm
PLACE_NEAR=U1800.AA16:2.54mm
=PP1V05_S0_PCH_VCCSSC
C2475 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AG33:2.54mm
=PP1V05_S0_PCH_VCCDIFFCLK
C2434 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF34:2.54mm
=PP3V3_S0_PCH_VCC3_3_HVCMOS
C2424 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.V33:2.54mm
=PP1V8_S0_PCH_VCCTX_LVDS
NO STUFF
L2407 0.1UH 0805
NO STUFF
C2400 22UF 20% 6.3V X5R-CERM-1 603
NOSTUFF
C2406 0.01UF 10% 16V X7R-CERM 0402
NO STUFF
C2408 0.01UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.AM37:2.54mm
PP1V8_S0_PCH_VCCTX_LVDS_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
R2401 0 5% 1/20W MF 201
PLACE_NEAR=U1800.AM37:2.54MM
=PP3V3_S5_PCH_VCCDSW
C2499 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.T16:2.54mm
=PP3V3_S0_PCH_VCC3_3_PCI
C2421 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.BH29:2.54mm
=PP1V05_S0_PCH_VCCIO_CLK
C2469 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF17:2.54mm
=PP3V3_S0_PCH_VCCADAC
R2450 0 5% 1/20W MF 201
PP3V3_S0_PCH_VCCA_DAC_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C2450 10UF 20% 6.3V X5R 603
C2451 0.1UF 10% 16V X7R-CERM 0402
C2455 0.01UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.U48:2.54mm
=PP3V3_SUS_PCH_VCC_SPI
C2442 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.V1:2.54mm
=PP3V3_S0_PCH_VCC3_3_SATA
C2423 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.AJ2:2.54mm
=PP1V05_S0_PCH_VCCIO_SATA
C2444 1UF 10% 6.3V CERM 402
C2452 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AH13:2.54mm
PLACE_NEAR=U1800.AC17:2.54mm
=PP3V3_SUS_PCH_VCCSUS_GPIO
C2476 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.P22:2.54mm
PCH VCCIO BYPASS
(PCH USB 1.05V PWR)
=PP1V05_S0_PCH_VCCIO_USB
C2446 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.P28:2.54mm
PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)
=PP3V3_SUS_PCH_VCCSUS_USB
C2484 0.1UF 10% 16V X7R-CERM 0402
C2413 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.P24:2.54mm
PLACE_NEAR=U1800.V24:2.54mm
=PP1V05_S0_PCH_VCCIO
C2401 10UF 20% 6.3V X5R 603
C2429 1UF 10% 6.3V CERM 402
C2414 1UF 10% 6.3V CERM 402
C2407 1UF 10% 6.3V CERM 402
C2463 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AN27:2.54mm
=PP3V3_S0_PCH_VCC3_3_CLK
R2451 1 5% 1/16W MF-LF 402
PP3V3_S0_PCH_VCC3_3_CLK_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
CRITICAL
L2451 10UH-0.12A-0.36OHM 0603
PP3V3_S0_PCH_VCC3_3_CLK_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=3.3V
C2453 10UF 20% 6.3V X5R 603
C2454 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.T38:2.54mm
PCH VCCSUSHDA BYPASS
=PP3V3R1V5_S0_PCH_VCCSUSHDA
C2441 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.P32:2.54mm
=PP1V05_S0_PCH_VCCASW
C2420 22UF 20% 6.3V X5R-CERM-1 603
C2428 22UF 20% 6.3V X5R-CERM-1 603
C2426 1UF 10% 6.3V CERM 402
C2456 1UF 10% 6.3V CERM 402
C2496 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AC27:2.54mm
=PP1V05_S0_PCH_VCCADPLL
R2490 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L2490 10UH-0.12A-0.36OHM 0603
PCH VCCADPLLA Filter
(PCH DPLLA PWR)
PP1V05_S0_PCH_VCCADPLLA_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
68 mA
CRITICAL
C2491 220UF 20% 2.5V TANT B16
NO STUFF
C2492 1UF 10% 6.3V CERM 402
(Z = 1.2MM, PLACE ON SHORT SIDE BEHIND PCH)
PLACE_NEAR=U1800.BD47:2.54MM
=PP1V8_S0_PCH_VCC_DFTERM
C2440 0.1UF 20% 10V CERM 402
PLACE_NEAR=U1800.AJ16:2.54mm
PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)
=PP1V05_S0_PCH_VCC_CORE
C2460 10UF 20% 6.3V X5R 603
C2481 1UF 10% 6.3V CERM 402
C2482 1UF 10% 6.3V CERM 402
C2483 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AG26:2.54mm
PLACE_NEAR=U1800.AD21:2.54mm
PLACE_NEAR=U1800.AG24:2.54mm
PLACE_NEAR=U1800.AJ27:2.54mm
R2491 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L2491 10UH-0.12A-0.36OHM 0603
PCH VCCADPLLB Filter
(PCH DPLLB PWR)
PP1V05_S0_PCH_VCCADPLLB_F
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
69 mA
CRITICAL
C2493 220UF 20% 2.5V TANT B16
NO STUFF
C2494 1UF 10% 6.3V CERM 402
(Z = 1.2MM, PLACE ON SHORT SIDE BEHIND PCH)
PLACE_NEAR=U1800.BF47:2.54MM
=PP1V05_S0_PCH_V_PROC_IO
C2416 4.7UF 20% 6.3V X5R 402
C2417 0.1UF 10% 16V X7R-CERM 0402
C2430 0.1UF 10% 16V X7R-CERM 0402
PLACE_NEAR=U1800.BJ8:2.54mm
=PP1V05_S0_PCH
CRITICAL
L2406 10UH-0.58A-0.35OHM 1098AS-SM
PP1V05_S0_PCH_VCCCLKDMI_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.05V
(Z = 1.2MM, PLACE ON SHORT SIDE BEHIND PCH)
R2415 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCCLKDMI_F
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.05V
C2411 10UF 20% 6.3V X5R 603
PLACE_NEAR=U1800.AB36:2.54mm
=PP1V05_S0_PCH_VCC_DMI
C2419 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AT20:2.54mm
PCH VCCIO BYPASS
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)
SYNC MASTER=D2 CLEAN
SYNC DATE=03/19/2012
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PCH DECOUPLING
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REVISION 4.18.0
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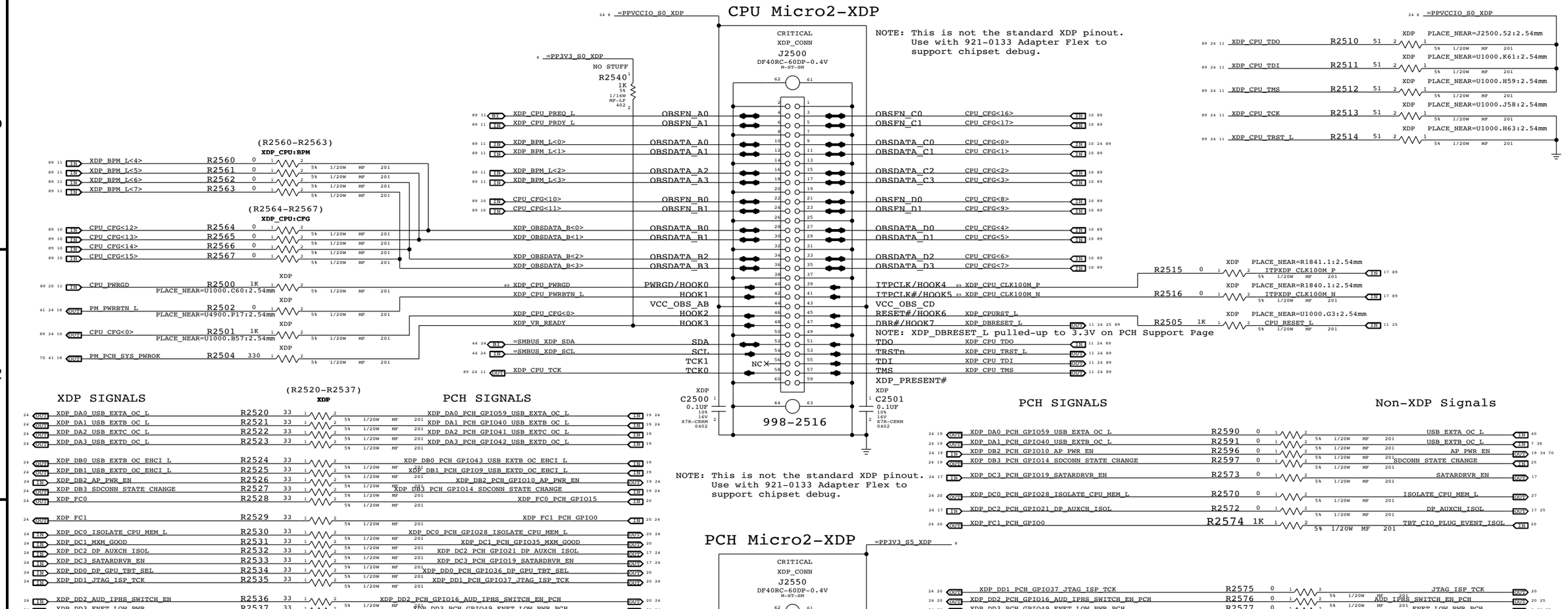
CPU Micro2-XDP



NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP SIGNALS

(R2520-R2537)

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

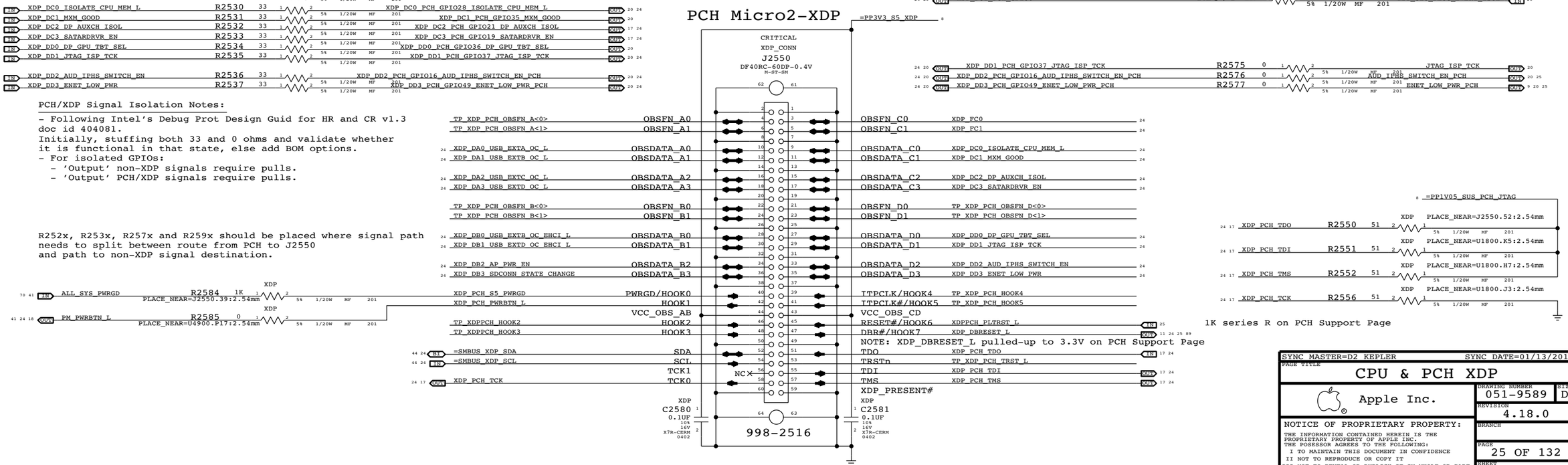
PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_PCH_GPIO0	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

Non-XDP Signals

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
  Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

1K series R on PCH Support Page

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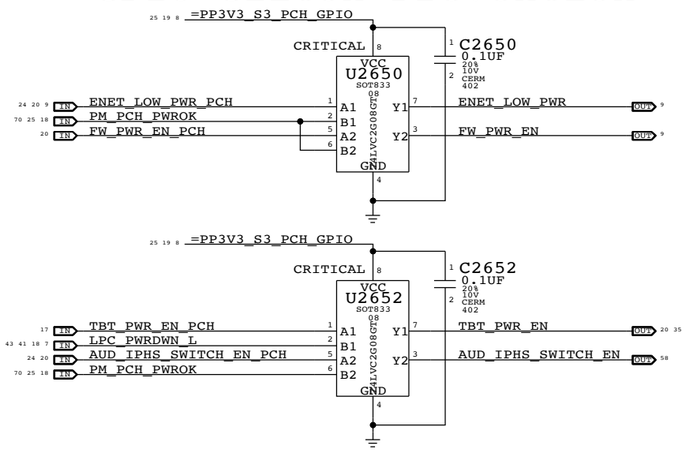
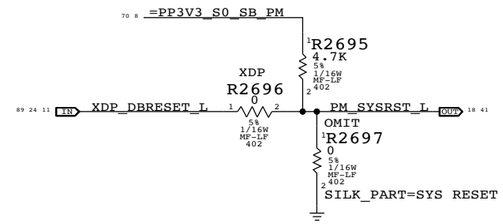
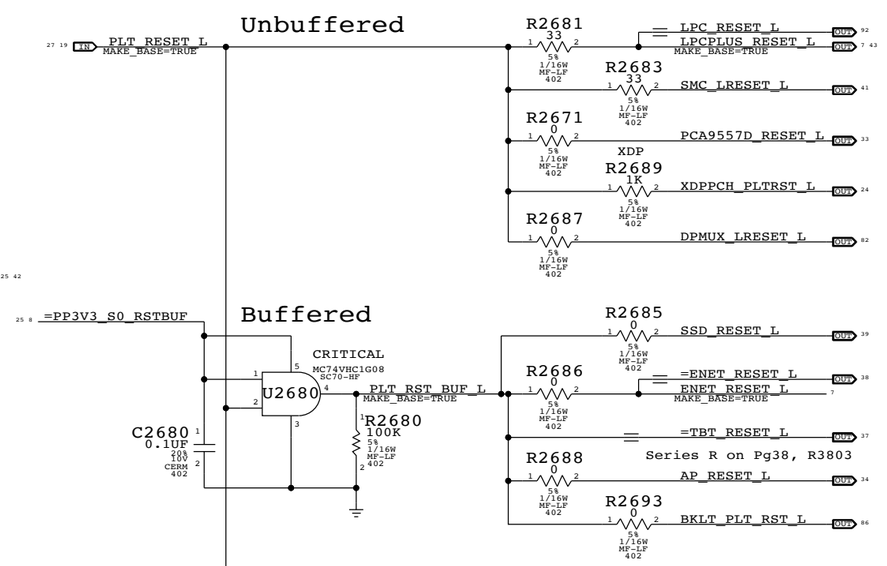
GPIO Glitch Prevention



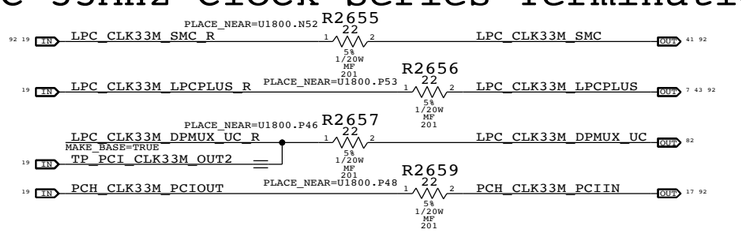
PCH Reset Button

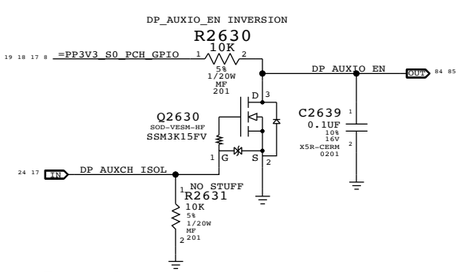


Platform Reset Connections



LPC 33MHz Clock Series Termination

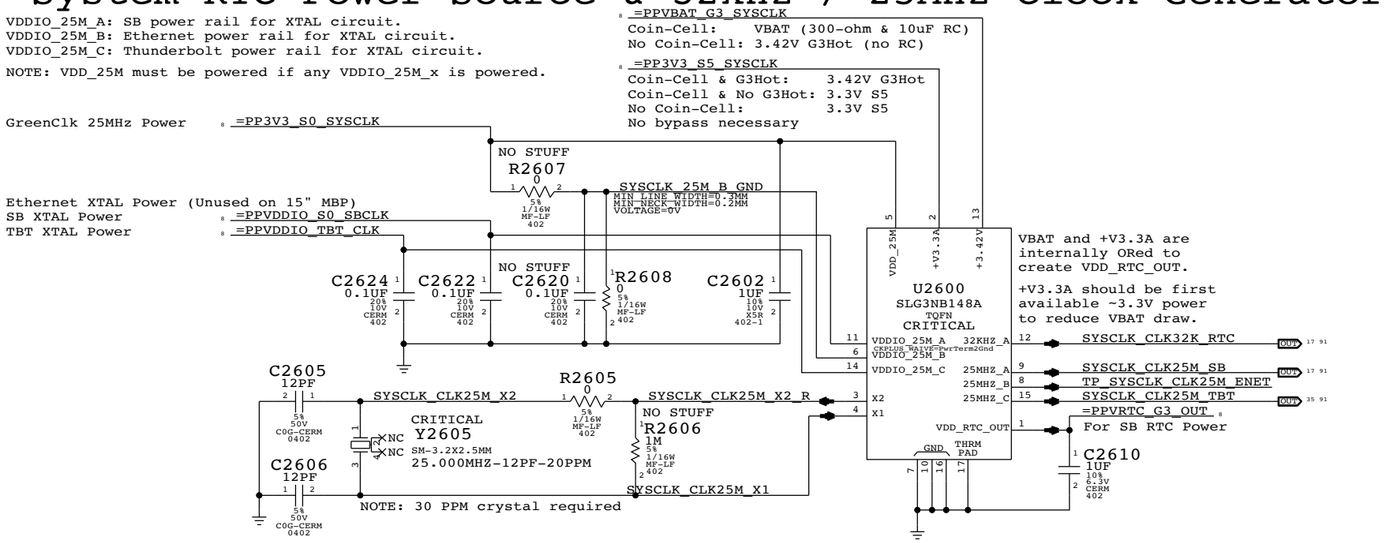




System RTC Power Source & 32kHz / 25MHz Clock Generator

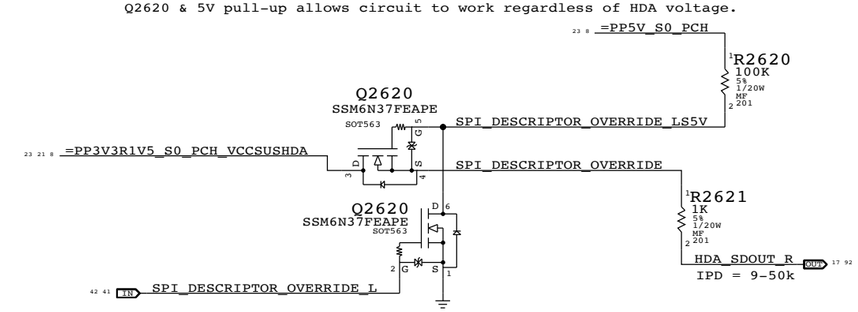
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=D2 KEPLER	SYNC DATE=01/13/2012
PAGE TITLE: Chipset Support	
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	REVISION: 4.18.0
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

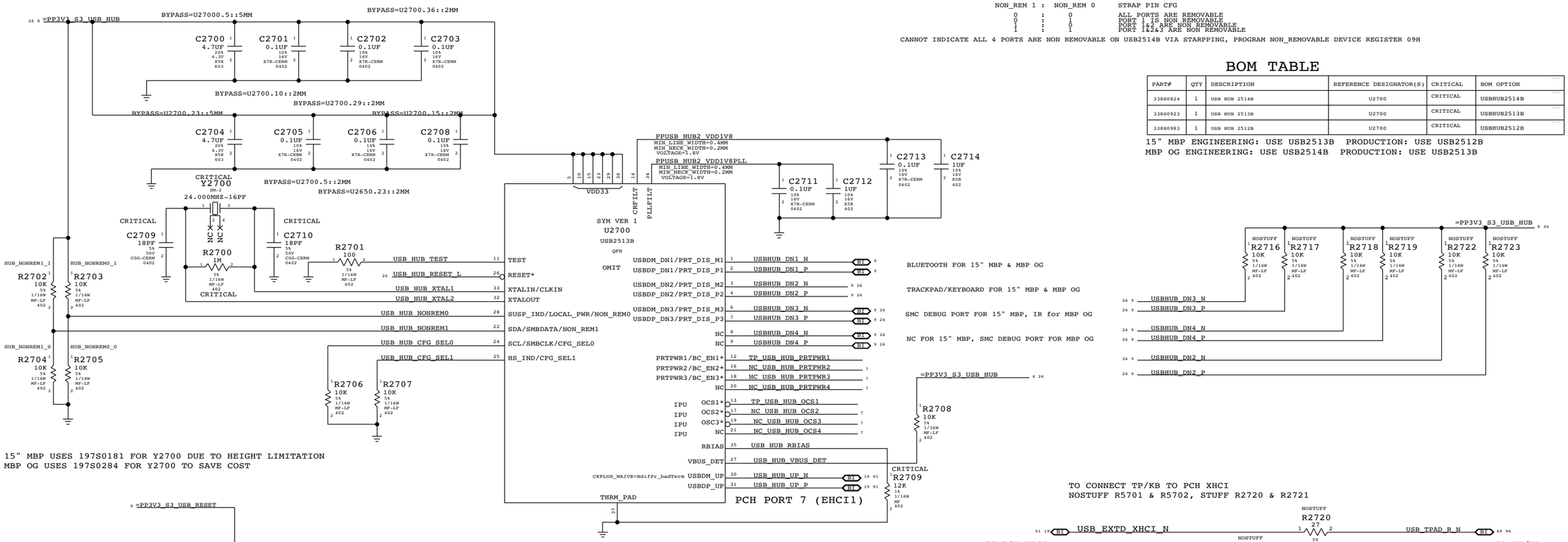
CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

BOM TABLE

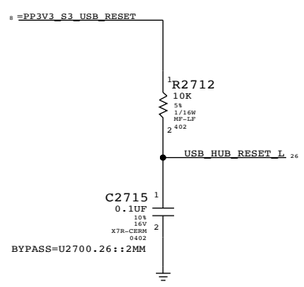
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B

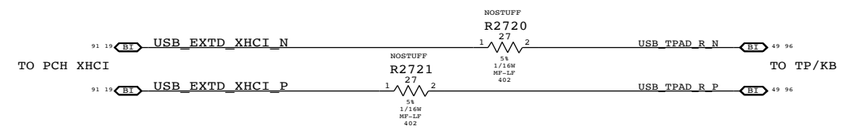
USB MUX FOR LS/FS INTERNAL DEVICES



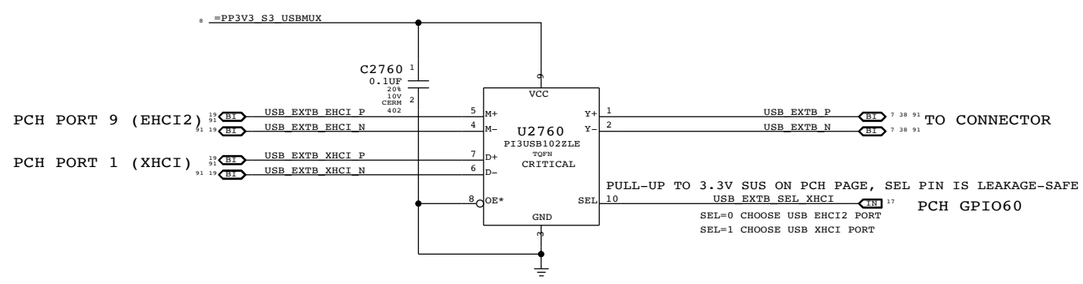
15" MBP USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
MBP OG USES 197S0284 FOR Y2700 TO SAVE COST



TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



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PAGE TITLE
USB HUB & MUX

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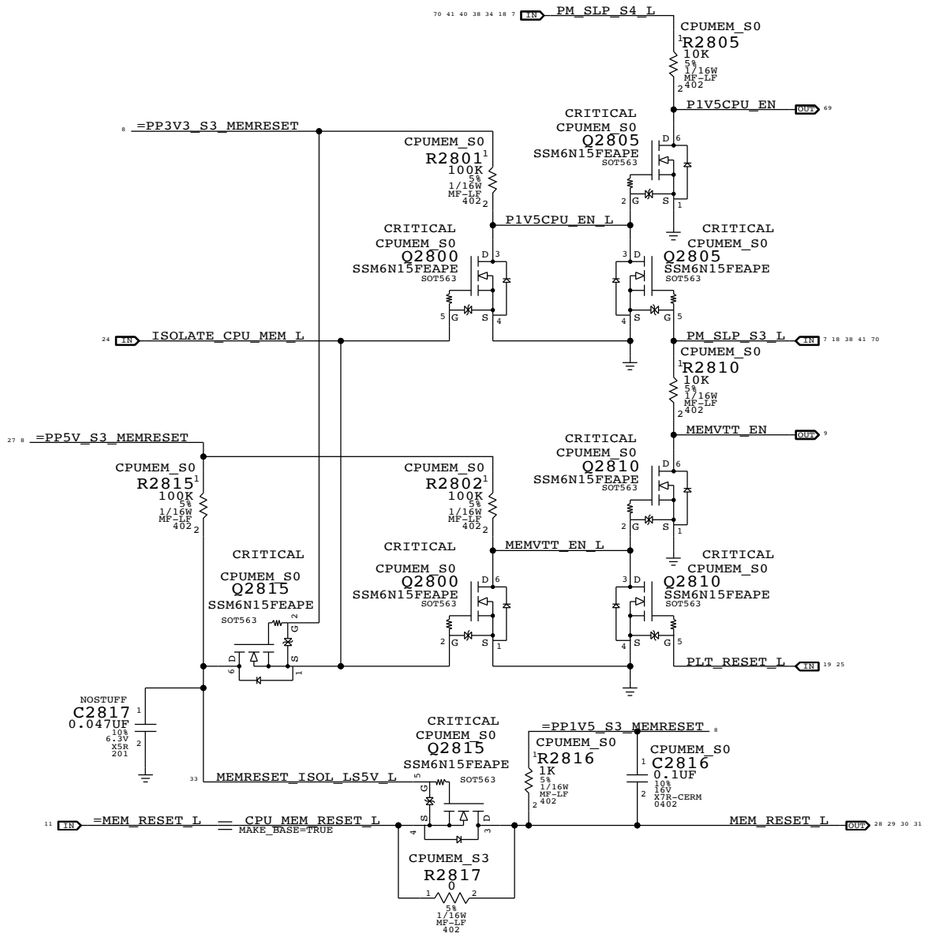
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

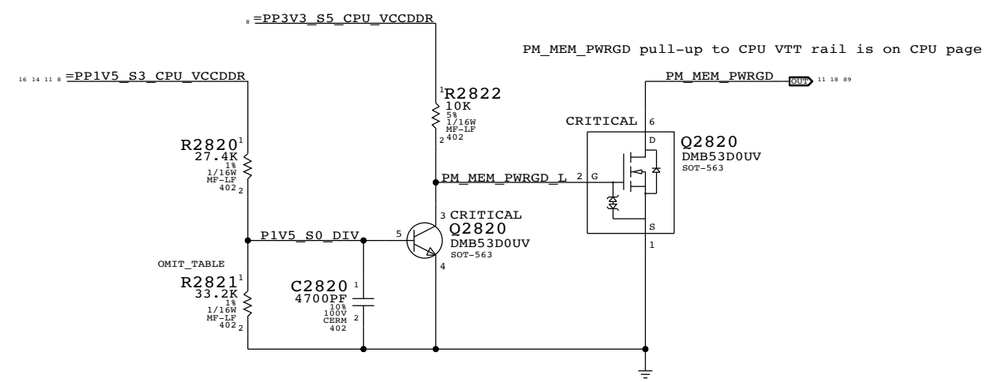
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



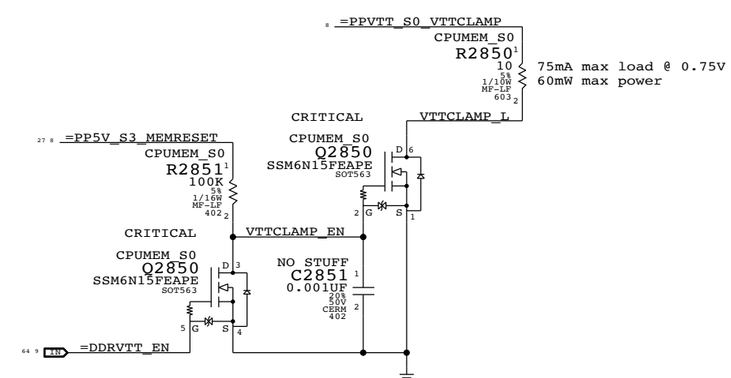
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES,MTL FILM,1/16W,33.2K,1,0402,SMD,LF	R2821		PPDDR:1V5
114S0376	1	RES,MTL FILM,1/16W,43.2K,1,0402,SMD,LF	R2821		PPDDR:1V35

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

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PAGE TITLE
CPU Memory S3 Support

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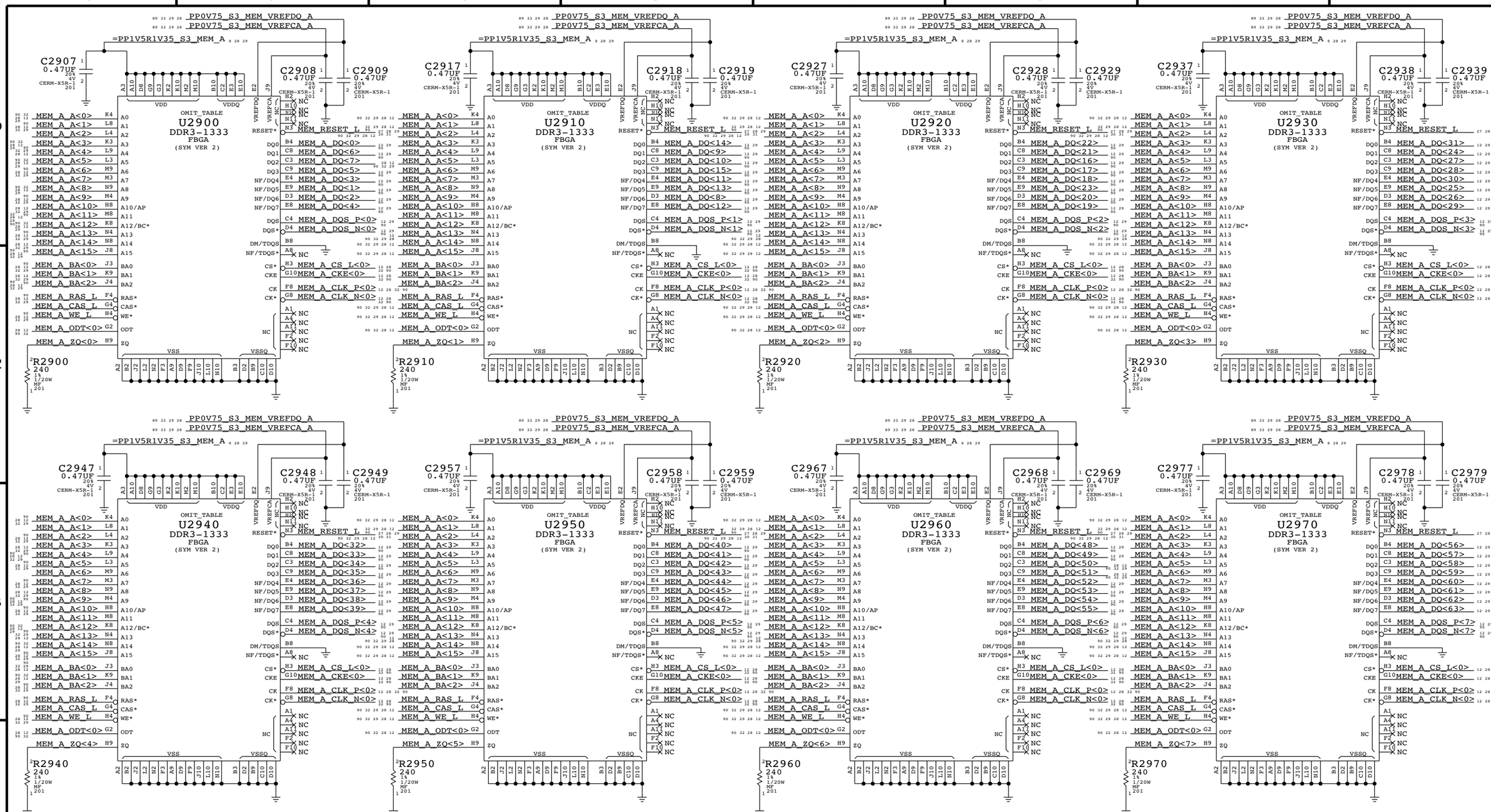

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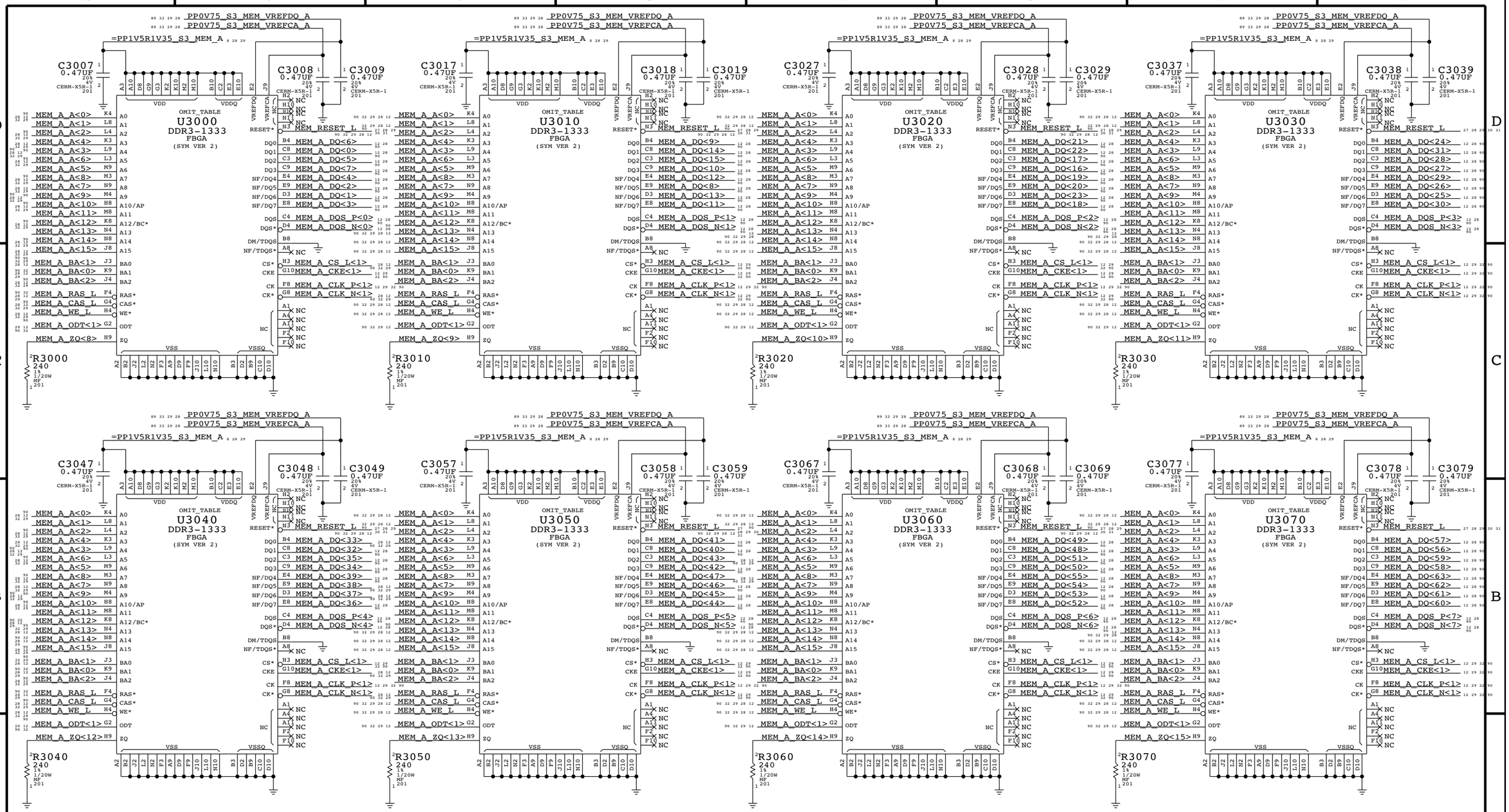

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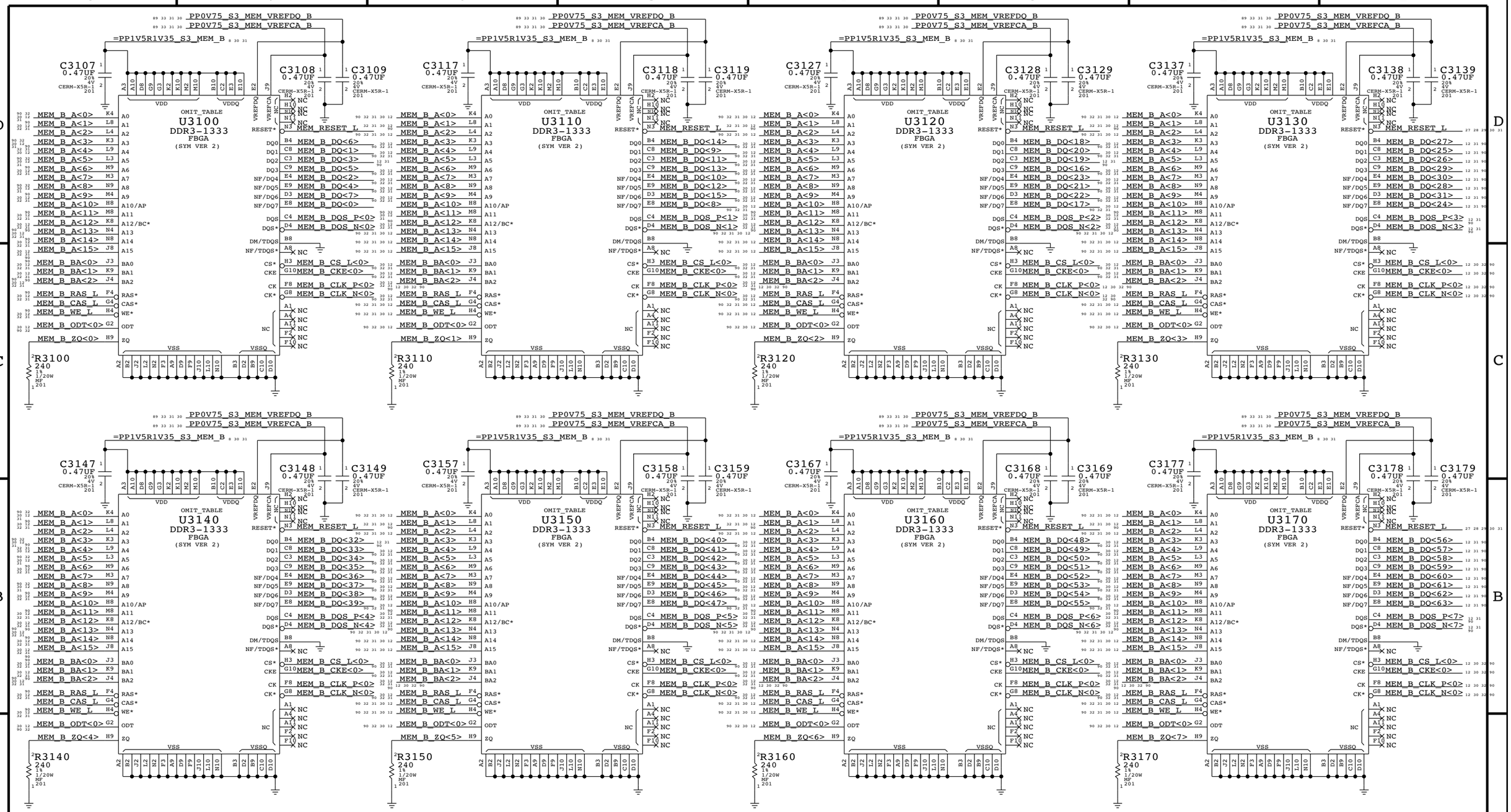

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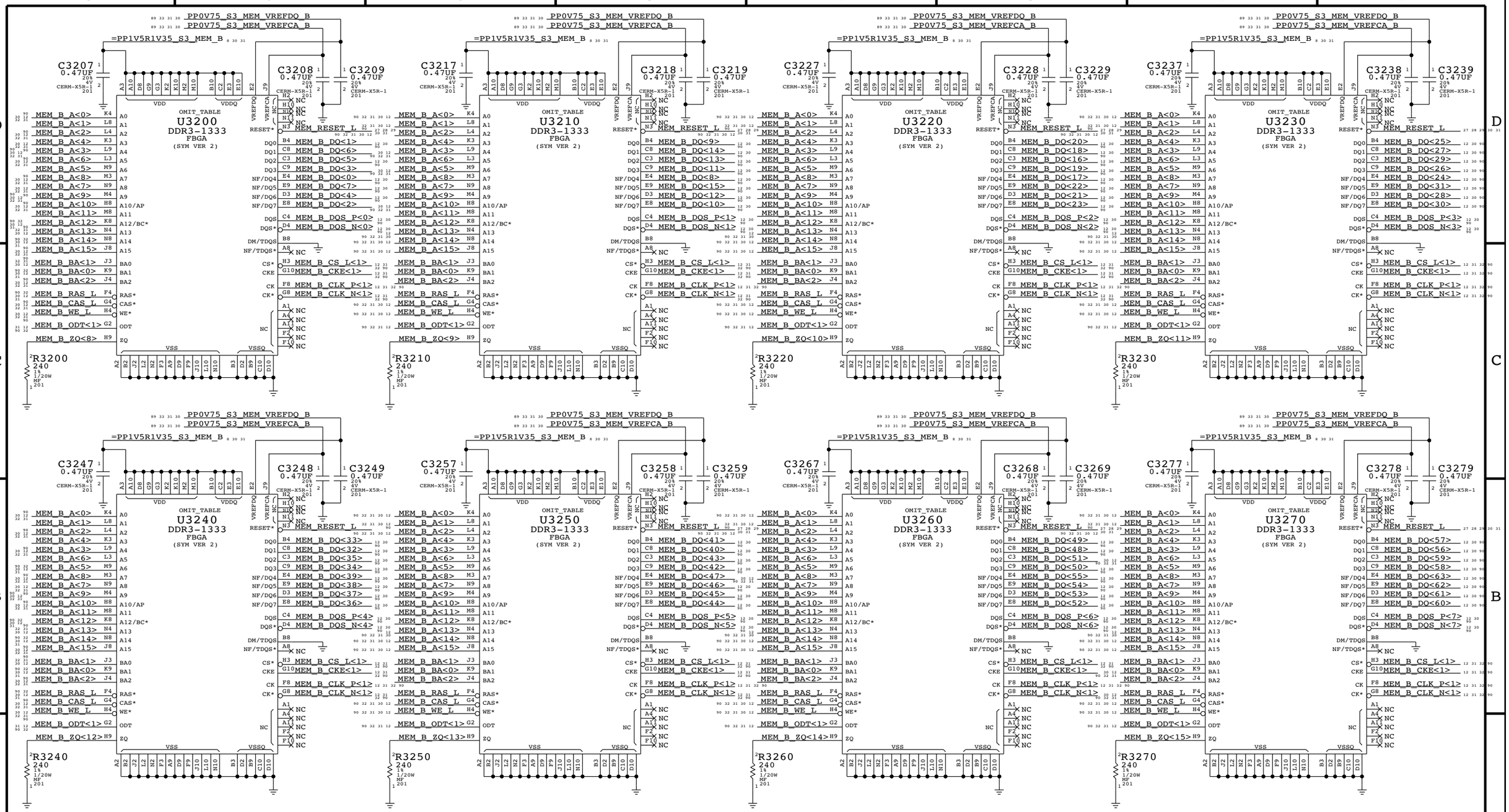

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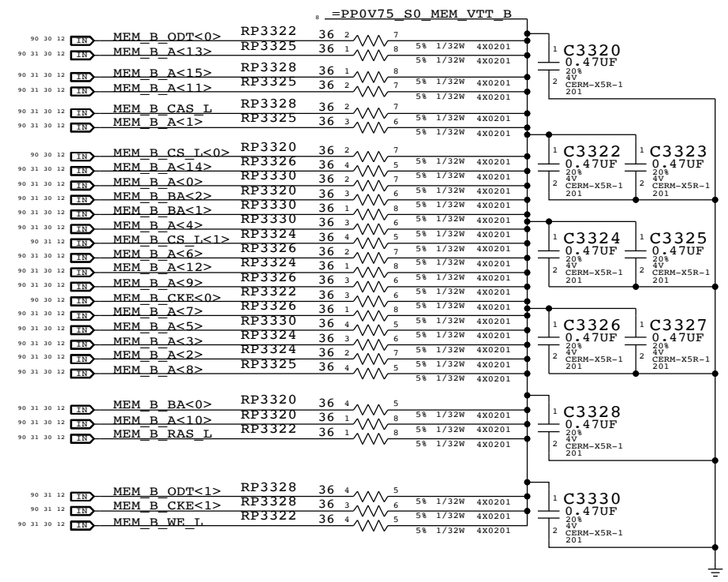
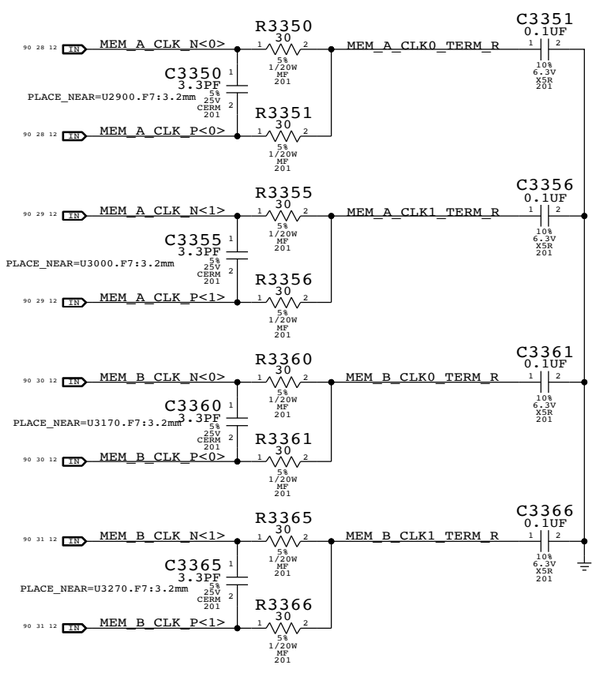
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



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DDR3 Termination

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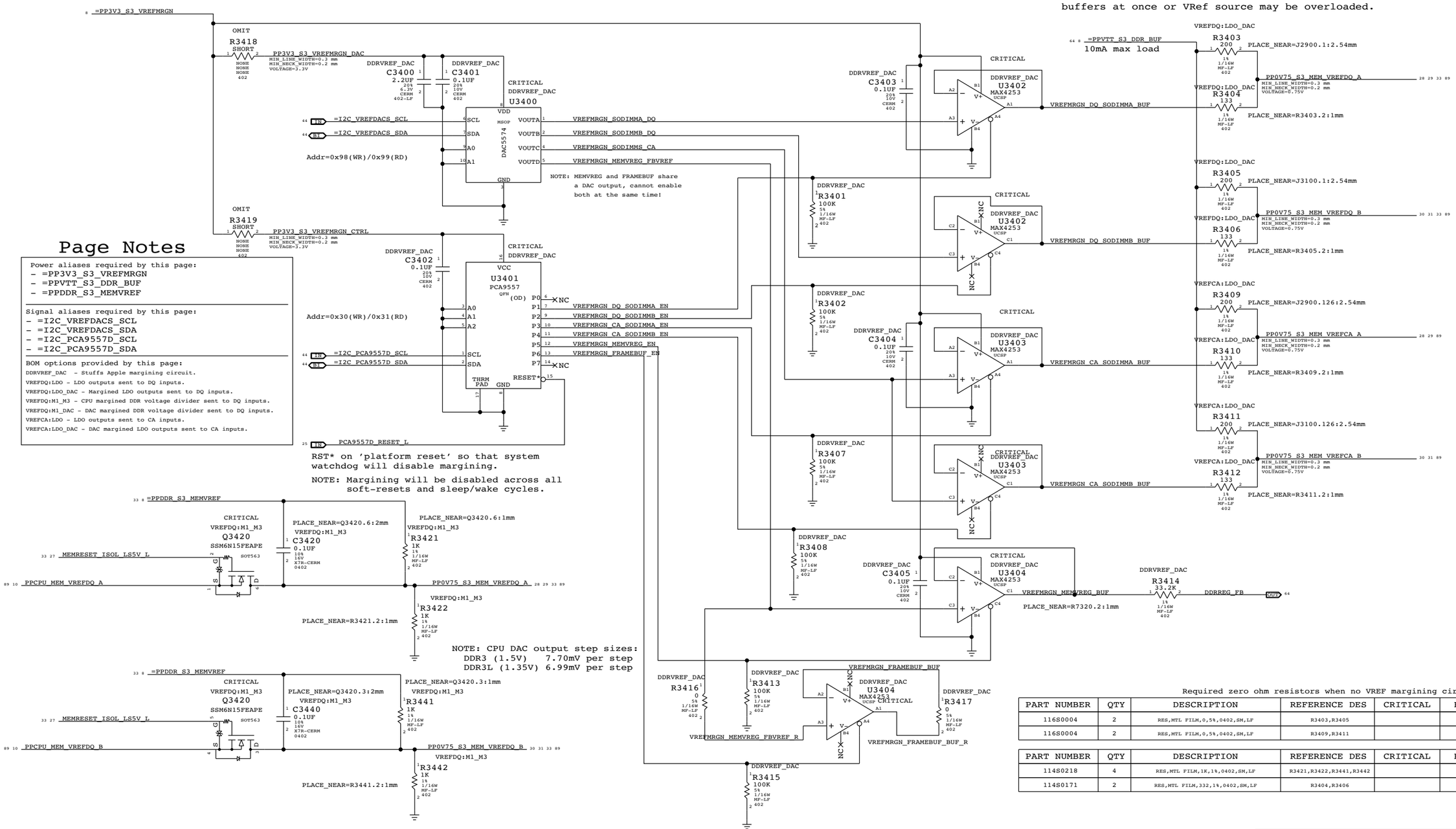

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

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DDR3/FRAMEBUF VREF MARGINING

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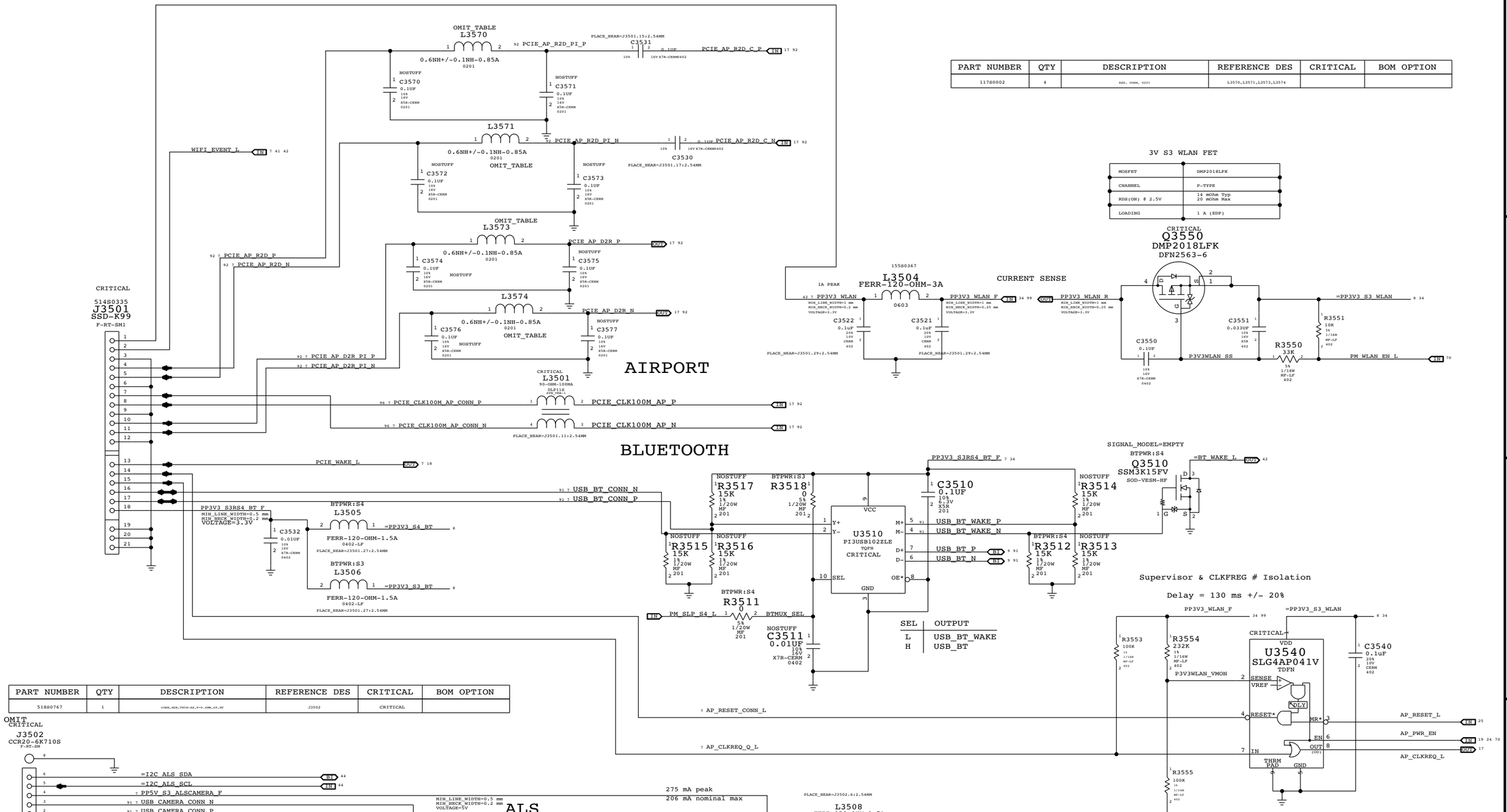
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	4	RES, 000M, 0201	L3570,L3571,L3573,L3574		



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0767	1	CONN,HDR,TWIN:AX,P=0.4MM,SP,RF	J3502	CRITICAL	

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X29/ALS/CAMERA CONNECTOR

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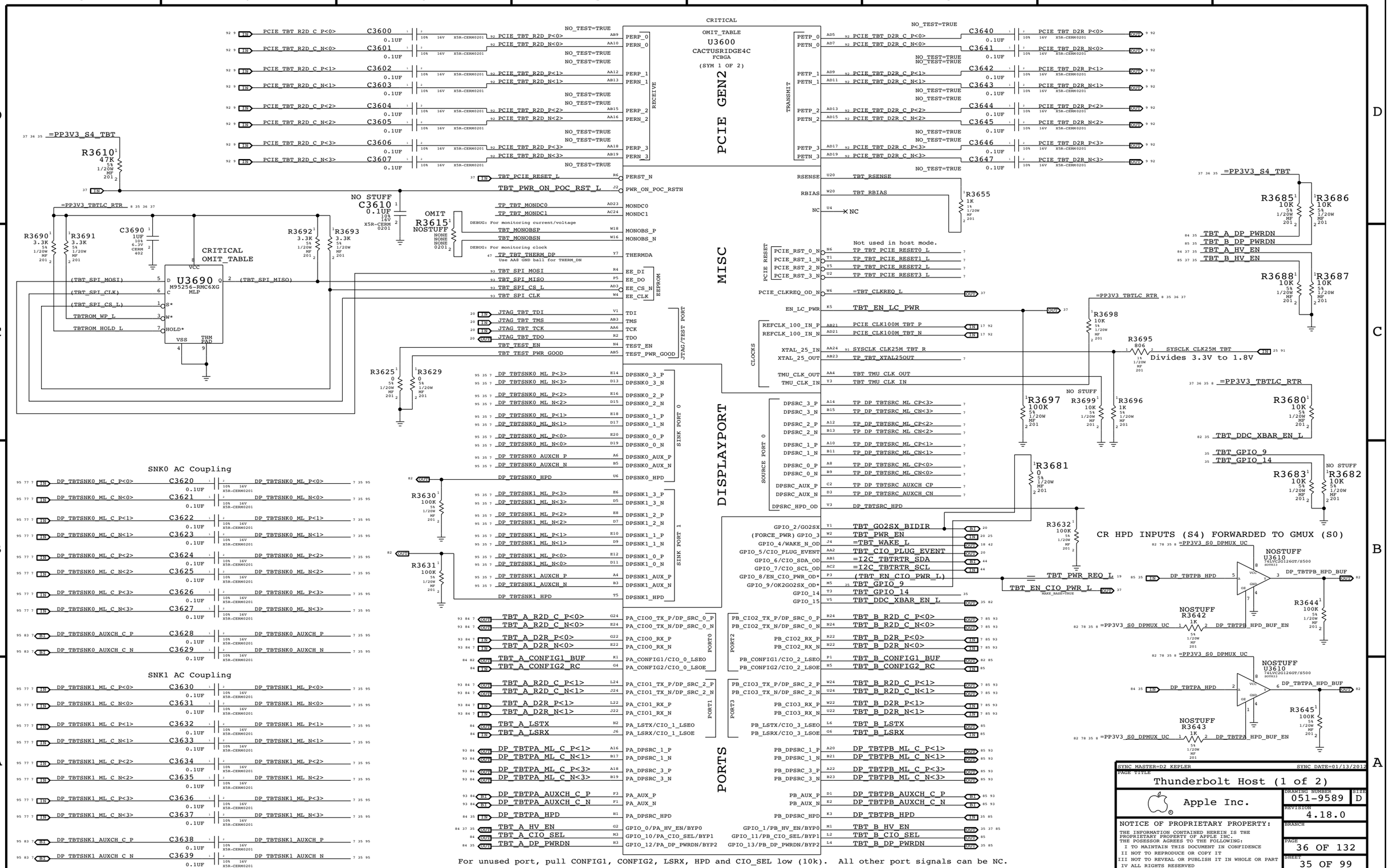
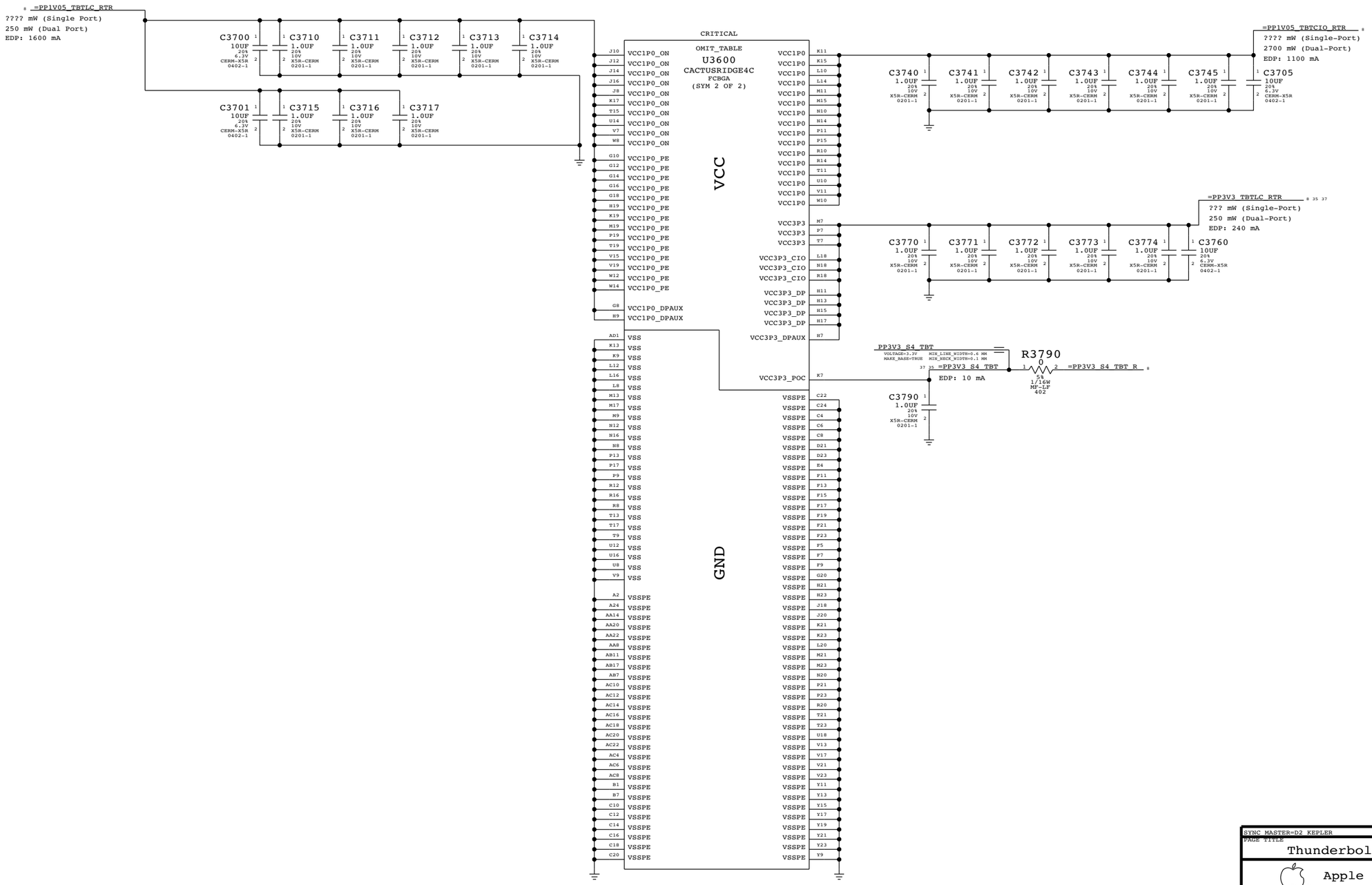


For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.



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Thunderbolt Host (2 of 2)

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Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL TBTBST:Y Q3880 SI8409DB BGA

=PPVIN_SW_TBTBST
8-13V Input Changes required for 2S.

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>

TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603

CRITICAL TBTBST:Y L3895 3.3UH-6.5A PIMB063T-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

TBTBST_SNS1
TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5

CRITICAL TBTBST:Y U3890 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_SNS2
XW3895 SM PLACE_NEAR=C3895.1:2 mm

TBTBST_VSNS
TBTBST:Y C3888 10PF 5% 50V C0G-CERM 0402
TBTBST:Y R3895 137K 1% 1/16W MF-LF 402 <Ra>
TBTBST_FBX
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/16W MF-LF 402 <Rb>

TBTBST:Y C3895 10UF 10% 25V X5R 1206-2
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
NO STUFF C3897 10UF 10% 25V X5R 805
=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 300KHz
TBTBST:Y C3899 0.001UF 10% 50V X7R-CERM 0402

TBTBST:Y C3890 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V C0G-CERM 0402
TBTBST:Y R3893 49.9K 1% 1/16W MF-LF 402
TBTBST_VC_RC
TBTBST:Y C3893 0.0033UF 10% 50V X7R-CERM 0402
TBTBST:Y R3894 28.7K 1% 1/16W MF-LF 402
TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

33UF-0.06OHM

TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBT_A_HV_EN
TBT_B_HV_EN

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
C3800 0.1UF 10% 16V X5R-CERM 0201
Q3840 SSM3K15FV SOD-VESM-HF
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
Platform (PCIe) Reset
=TBT_RESET_L
TBT_CLKREQ_L
Pull-ups provided by SB page.

CRITICAL U3800 SLG4AP016V TDFN
VDD, SENSE, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD
0.7V
DLY = 60 ms +/- 20%

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
TBTBST:Y R3888 330K 5% 1/16W MF-LF 402
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/16W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
CRITICAL U3830 TPS3808 QFN
VDD, SENSE, CT, GND, THRM PAD, RESET*, MR*
Pull-up: R3610
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
TBTPOCRST_MR_L
C3831 0.0047UF 10% 25V CERM 0402
C3830 0.1UF 10% 25V X5R 402
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
Q3825 SSM6N37FEAPE SOT563
C3825 330PF 10% 16V X7R-CERM 0201
=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP
A2, B2, VIN, ON, A1, B1, VOUT, C1, GND, CRITICAL
=PP3V3_TBTLC_FET
Max Current = 2A (85C)
C3810 1UF 20% 6.3V X5R 0201
R3811 36.5K 1% 1/20W MF 201
TBT_EN_LC_3V3
C3811 1UF 10% 6.3V CERM 402
TBT_EN_LC_ISOL

U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

1.05V TBT "LC" Switch

R3816 0 5% 1/20W MF 201
TBT_EN_LC_1V05
=PP1V05_S0_P1V05TBTFET
U3815 TPS22924 CSP
A2, B2, VIN, ON, A1, B1, VOUT, C1, GND, CRITICAL
=PP1V05_TBTLC_FET
Max Current = 2A (85C)
C3815 1UF 20% 6.3V X5R 0201
NOSTUFF C3816 1UF 10% 6.3V CERM 402
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V

U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3825 SSM6N37FEAPE SOT563
U3820 TPS22920 CSP
A2, B2, C2, VIN, ON, A1, B1, C1, VOUT, GND, CRITICAL
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
C3820 1UF 20% 6.3V X5R 0201
TBT_EN_CIO_PWR_L

U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012
PAGE TITLE: Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D
REVISION 4.18.0
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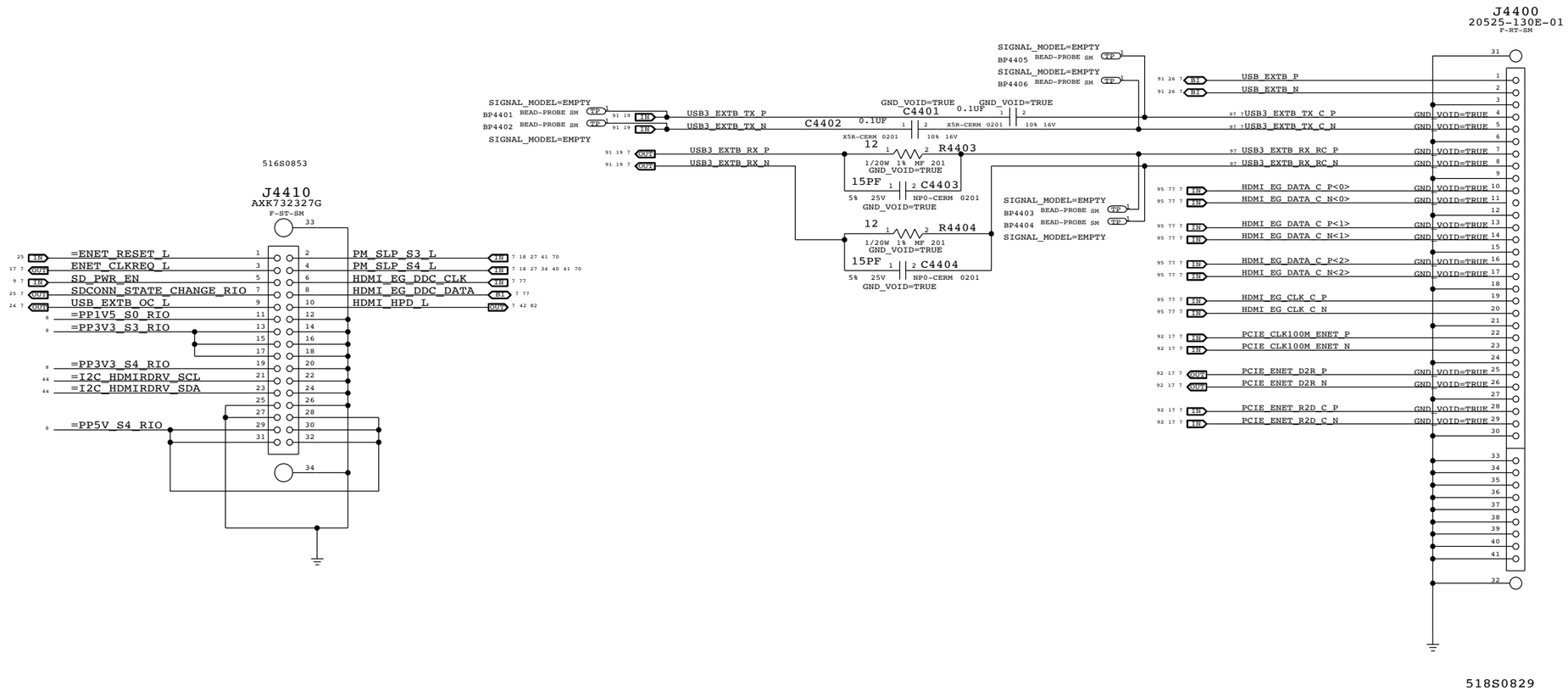

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

RIO CONNECTOR

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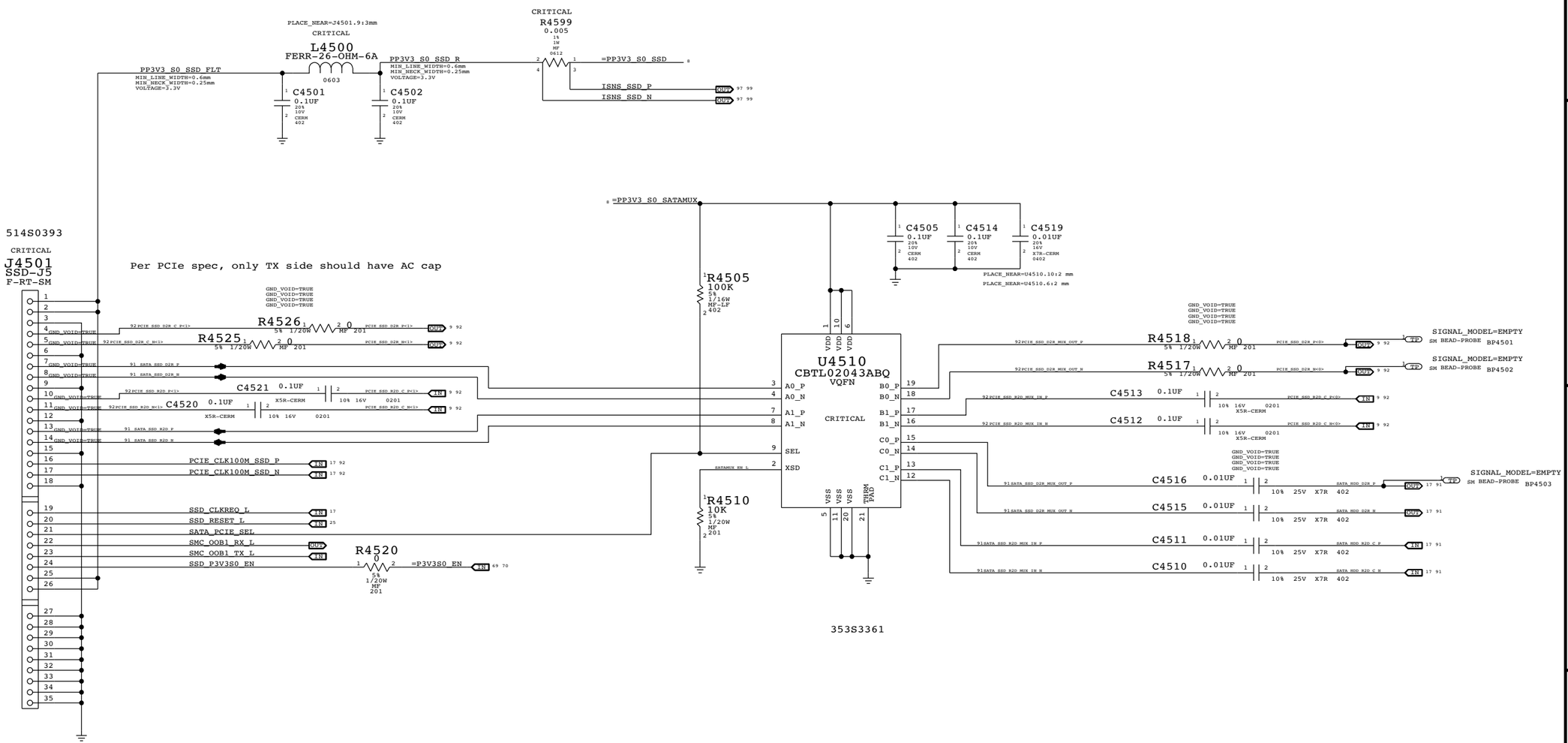

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=D2 KEPLER	SYNC DATE=01/13/2012
PAGE TITLE: SSD CONNECTOR	
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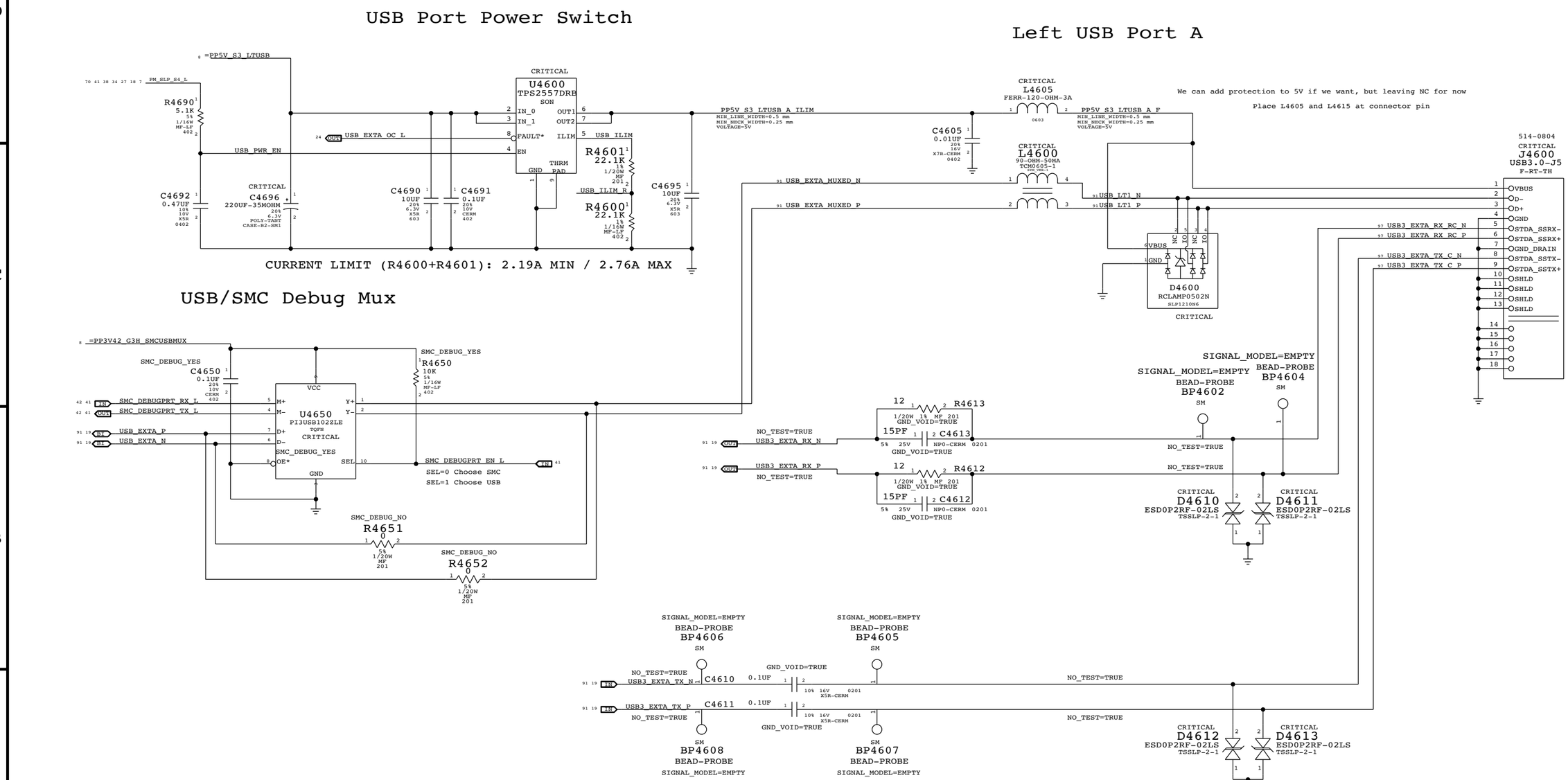

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PAGE TITLE

USB 3.0 CONNECTORS

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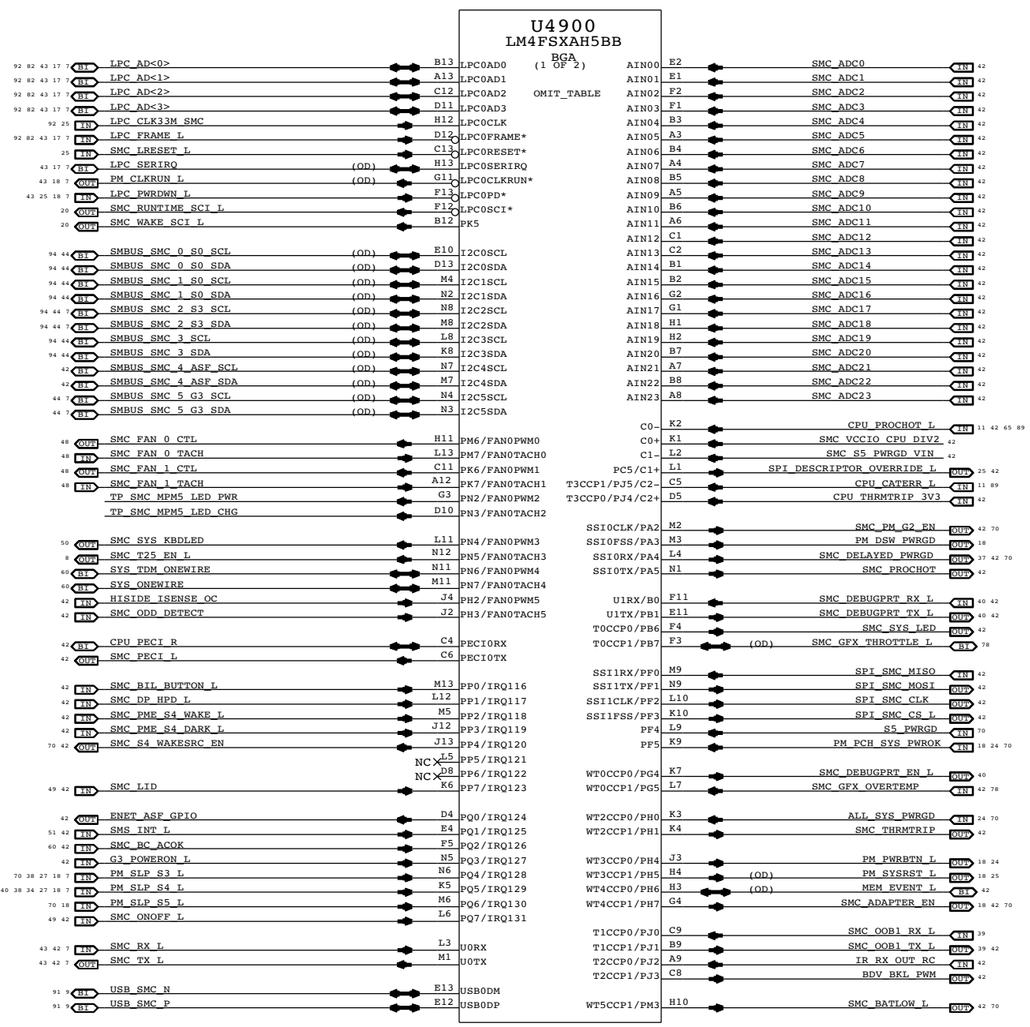
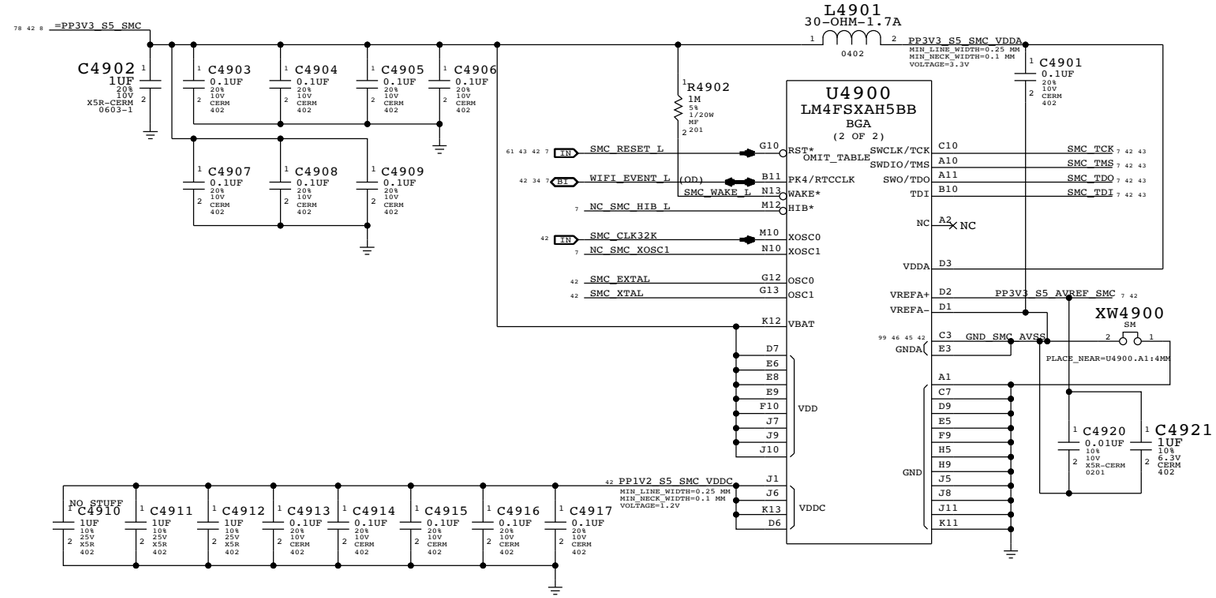
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

SMC

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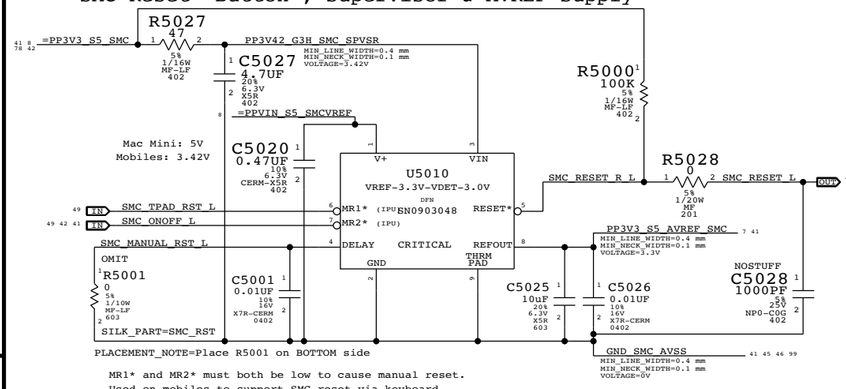
SMC Reset "Button", Supervisor & AVREF Supply

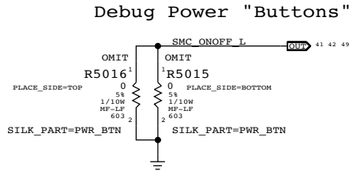


PLACEMENT_NOTE=Place R5001 on BOTTOM side

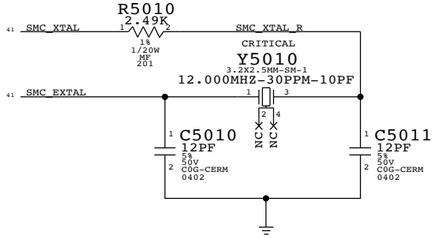
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



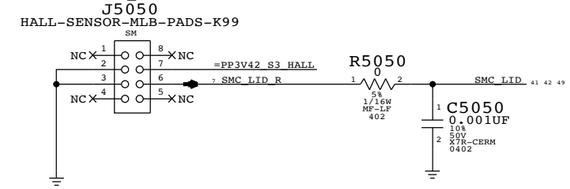
SMC Crystal Circuit



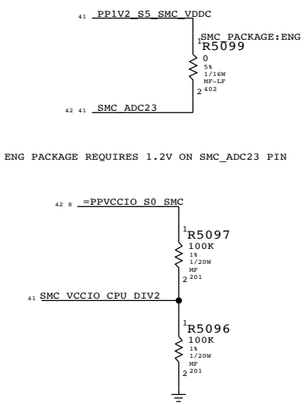
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

Hall Effect pads

APN: 998-3029
OMIT_TABLE

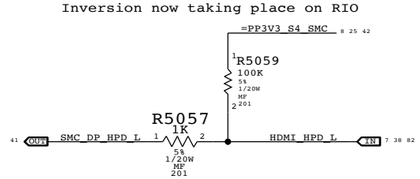


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	

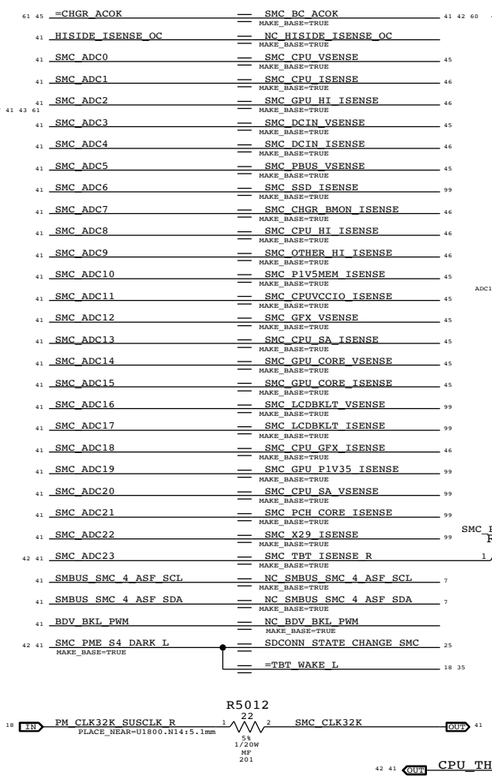


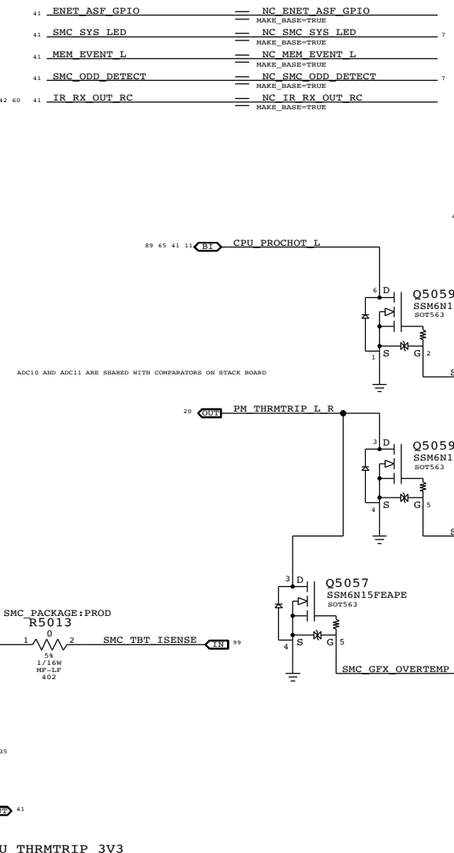
HDMI HPD ESD PROTECTION

Inversion now taking place on RIO

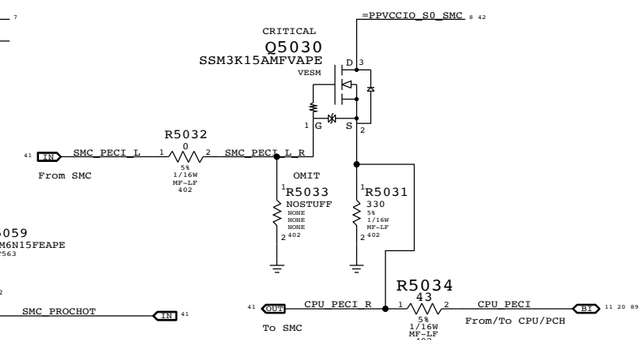


1K for ESD protection

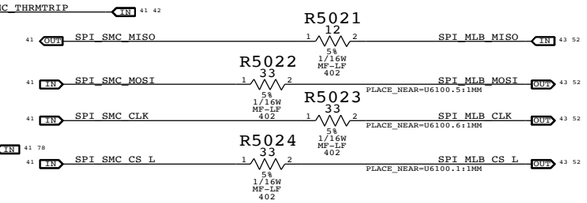


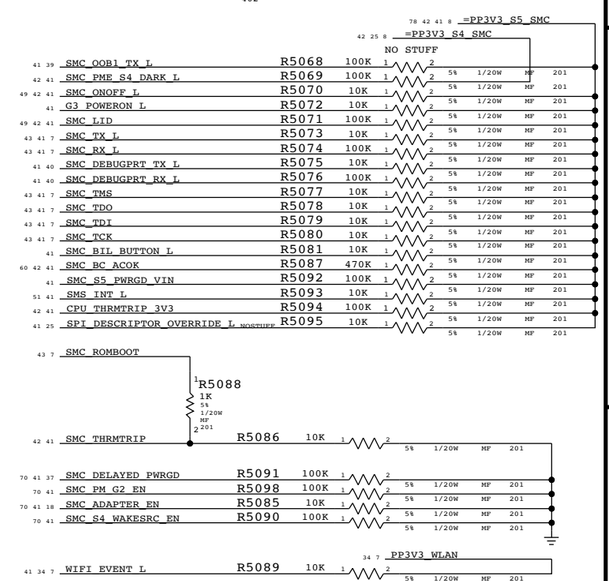


SMC12 PECI SUPPORT

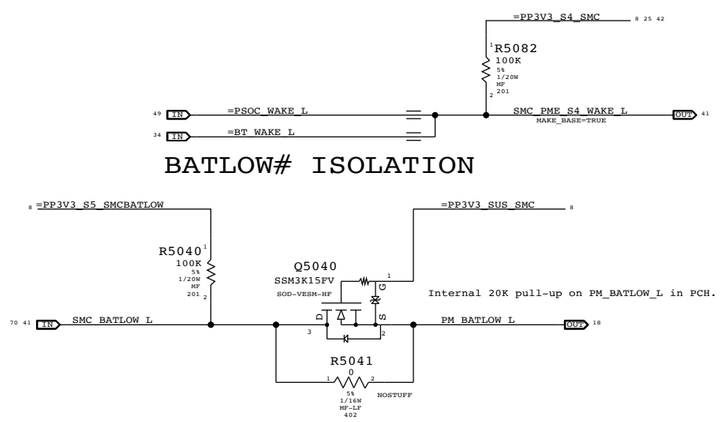


SMC12 SPI SUPPORT





BATLOW# ISOLATION



SYNC MASTER=D2 KEPLER — SYNC DATE=01/13/2012

PAGE TITLE: SMC Support

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DRAWING NUMBER: 051-9589 — SIZE: D

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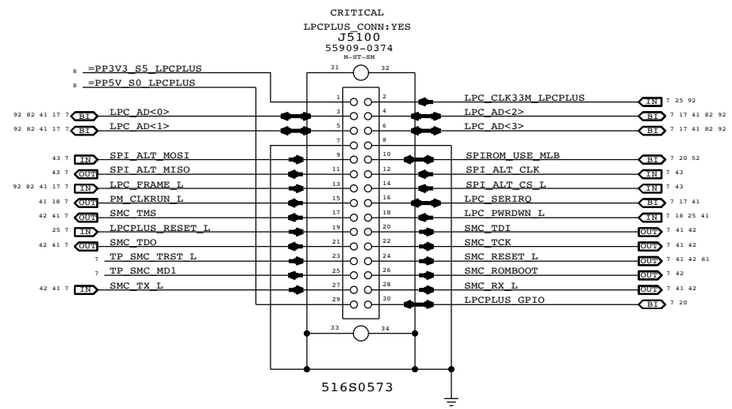
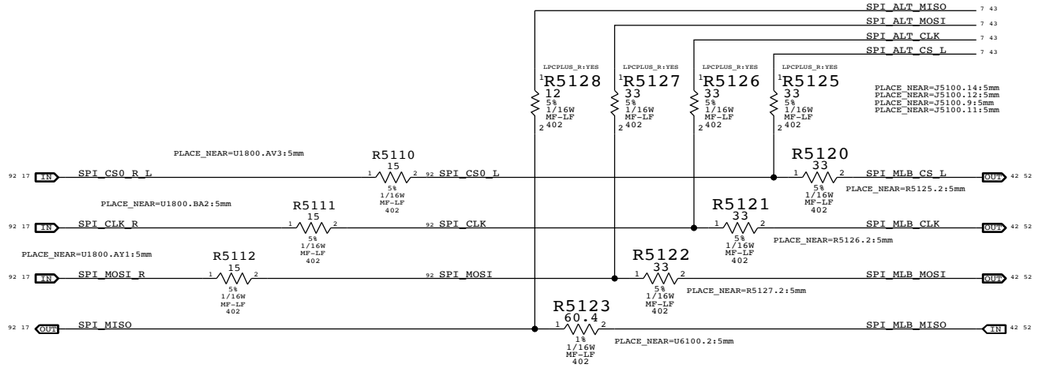
LPC+SPI Connector



SPI Bus Series Termination



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LPC+SPI Debug Connector

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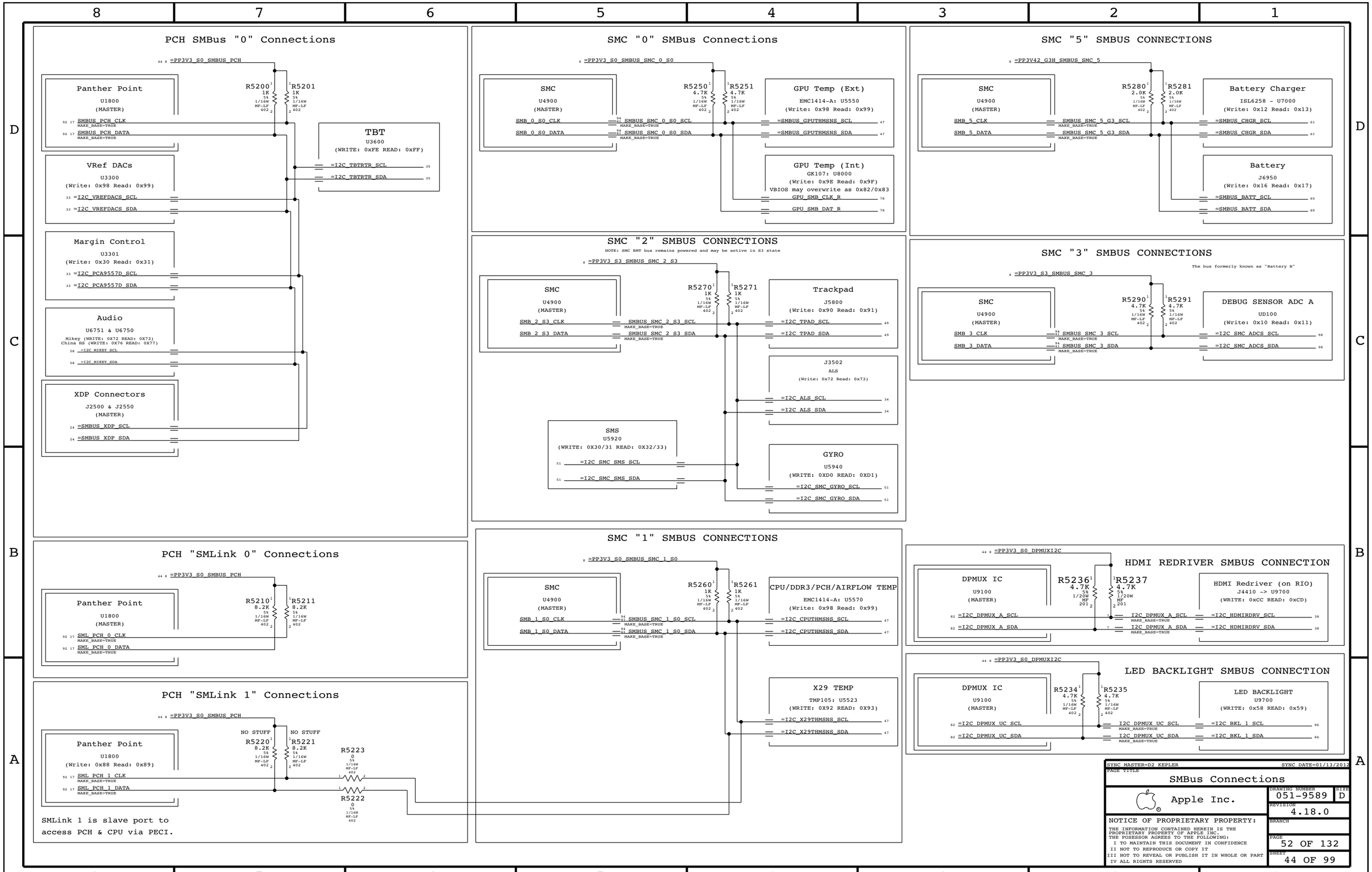
PCH SMBus "0" Connections
=PP3V3_S0_SMBUS_PCH
Panther Point
U1800
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
MAKE_BASE=TRUE
R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402
TBT
U3600
(WRITE: 0xFE READ: 0xFF)
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA
VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
Audio
U6751 & U6750
Mikey (WRITE: 0X72 READ: 0X73)
China HS (WRITE: 0X76 READ: 0X77)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
XDP Connectors
J2500 & J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA
SMC "0" SMBus Connections
=PP3V3_S0_SMBUS_SMC_0_S0
SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE
R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402
GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA
GPU Temp (Int)
GK107: U8000
(Write: 0x9E Read: 0x9F)
VBIOS may overwrite as 0x82/0x83
GPU_SMB_CLK_R
GPU_SMB_DAT_R
SMC "5" SMBUS CONNECTIONS
=PP3V42_G3H_SMBUS_SMC_5
SMC
U4900
(MASTER)
SMB_5_CLK
SMB_5_DATA
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE
R5280 2.0K 5% 1/16W MF 402
R5281 2.0K 5% 1/16W MF 402
Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
Battery
J6950
(Write: 0x16 Read: 0x17)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA
SMC "2" SMBUS CONNECTIONS
NOTE: SMC RMT bus remains powered and may be active in S3 state
=PP3V3_S3_SMBUS_SMC_2_S3
SMC
U4900
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
MAKE_BASE=TRUE
R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402
Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA
J3502
ALS
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA
SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
=I2C_SMC_SMS_SCL
=I2C_SMC_SMS_SDA
GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
=I2C_SMC_GYRO_SCL
=I2C_SMC_GYRO_SDA
SMC "3" SMBUS CONNECTIONS
The bus formerly known as "Battery B"
=PP3V3_S3_SMBUS_SMC_3
SMC
U4900
(MASTER)
SMB_3_CLK
SMB_3_DATA
SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA
MAKE_BASE=TRUE
R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402
DEBUG SENSOR ADC A
UD100
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA
PCH "SMLink 0" Connections
=PP3V3_S0_SMBUS_PCH
Panther Point
U1800
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
MAKE_BASE=TRUE
R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402
SMC "1" SMBUS CONNECTIONS
=PP3V3_S0_SMBUS_SMC_1_S0
SMC
U4900
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE
R5260 1K 5% 1/16W MF-LF 402
R5261 1K 5% 1/16W MF-LF 402
CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA
X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA
HDMI REDRIVER SMBUS CONNECTION
=PP3V3_S0_DPMUXI2C
DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_A_SCL
=I2C_DPMUX_A_SDA
R5236 4.7K 5% 1/20W MF 201
R5237 4.7K 5% 1/20W MF 201
I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA
MAKE_BASE=TRUE
HDMI Redriver (on RIO)
J4410 -> U9700
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL
=I2C_HDMIRDRV_SDA
LED BACKLIGHT SMBUS CONNECTION
=PP3V3_S0_DPMUXI2C
DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_UC_SCL
=I2C_DPMUX_UC_SDA
R5234 4.7K 5% 1/16W MF-LF 402
R5235 4.7K 5% 1/16W MF-LF 402
I2C_DPMUX_UC_SCL
I2C_DPMUX_UC_SDA
MAKE_BASE=TRUE
LED BACKLIGHT
U9700
(WRITE: 0x58 READ: 0x59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA
PCH "SMLink 1" Connections
=PP3V3_S0_SMBUS_PCH
Panther Point
U1800
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA
MAKE_BASE=TRUE
NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
R5221 8.2K 5% 1/16W MF-LF 402
R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402
SMLink 1 is slave port to
access PCH & CPU via PECI.
SYNC MASTER=D2 KEPLER
SYNC DATE=01/13/2012
PAGE TITLE
SMBus Connections
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
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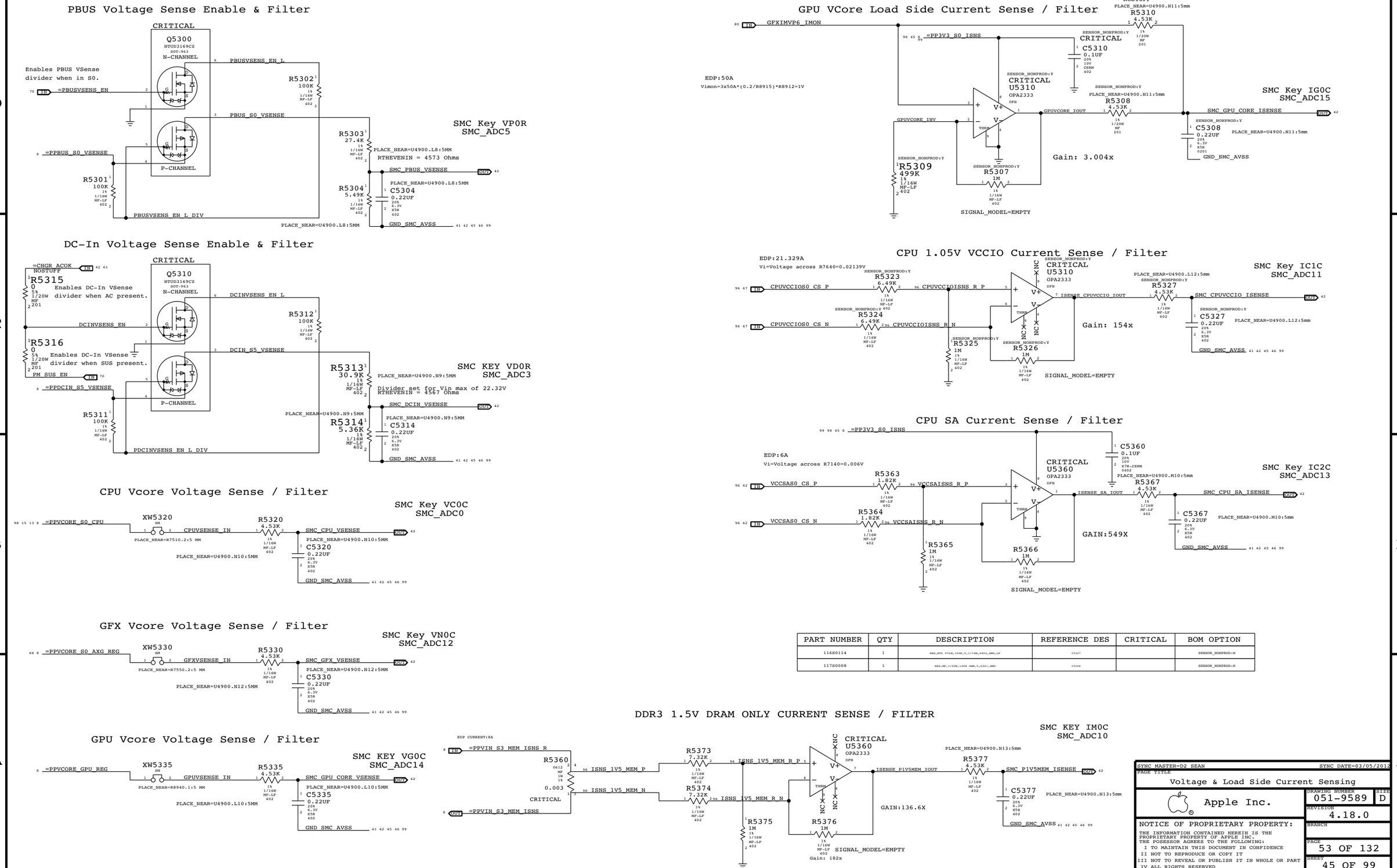

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	1	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	C5327		SENSOR_NONPROD:N
11780008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5309		SENSOR_NONPROD:N

SYNC MASTER=D2 SEAN SYNC DATE=03/05/2013

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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PAGE: 53 OF 132

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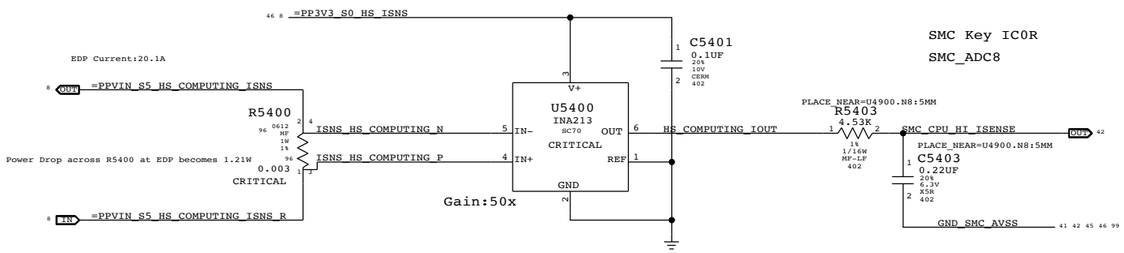
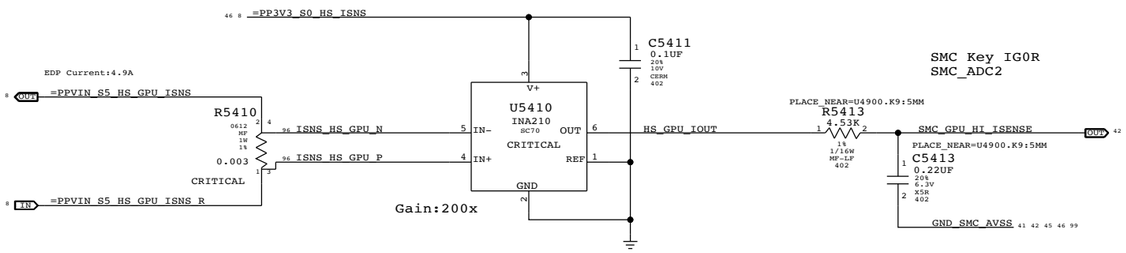
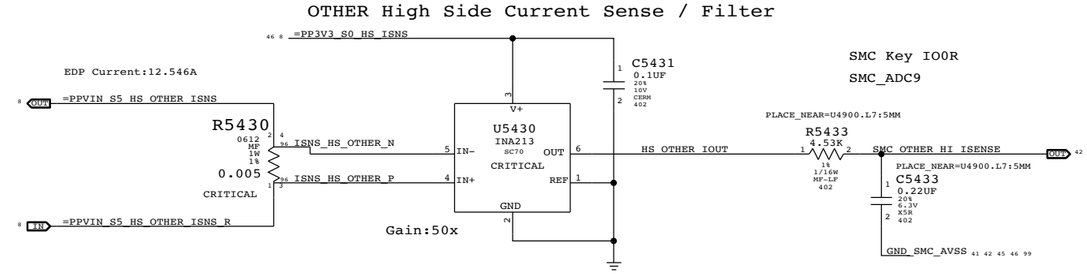
COMPUTING High Side Current Sense / Filter



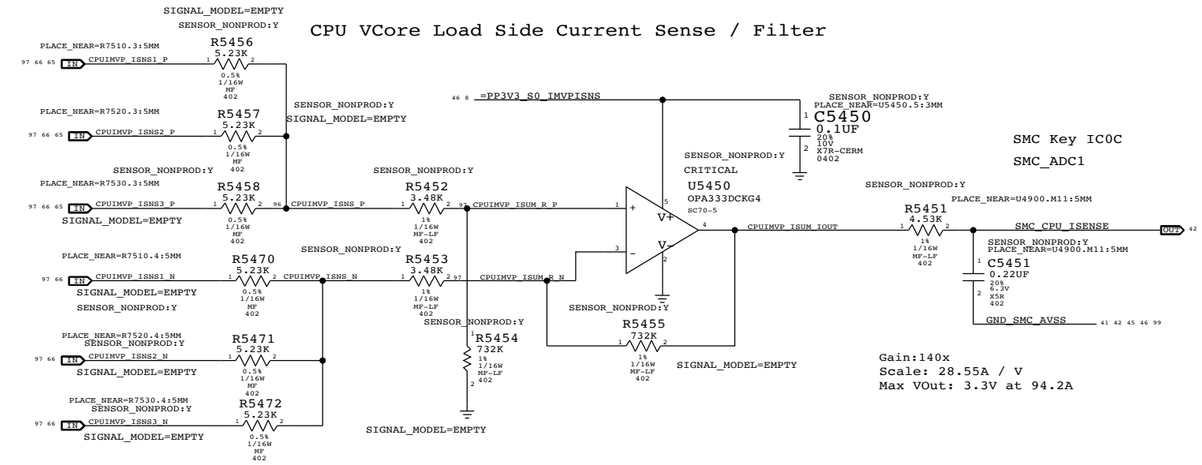
GRAPHICS High Side Current Sense / Filter



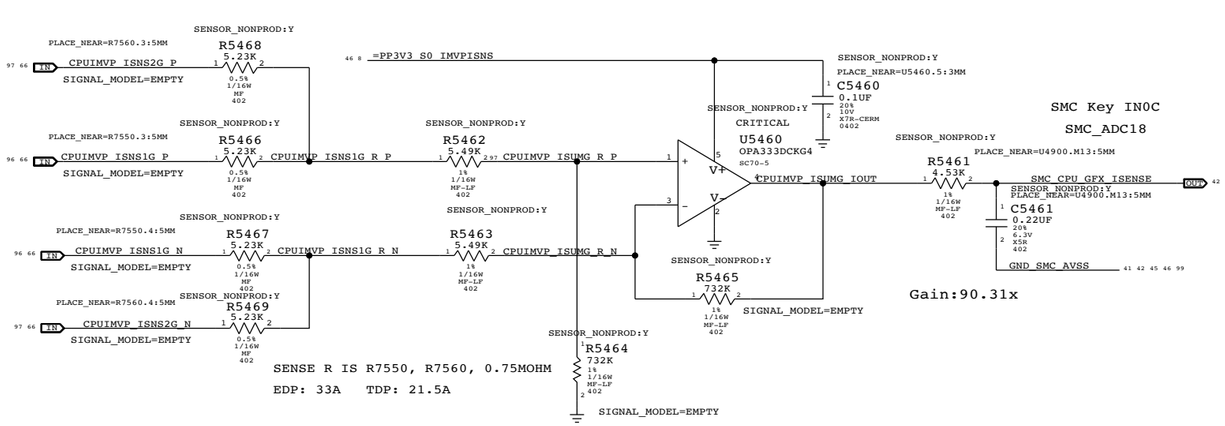
OTHER High Side Current Sense / Filter



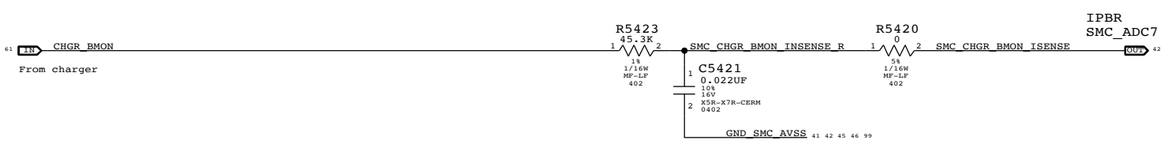
CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter

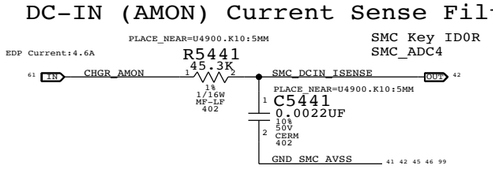


CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	2	RES,MFL FILM,100K,5,1/16W,0402,SMD,LF	C5451,C5461		SENSOR_NONPROD:N

DC-IN (AMON) Current Sense Filter



SYNC MASTER=D2 SEAN SYNC DATE=03/05/2013

PAGE TITLE

High Side and CPU/AXG Current Sensing

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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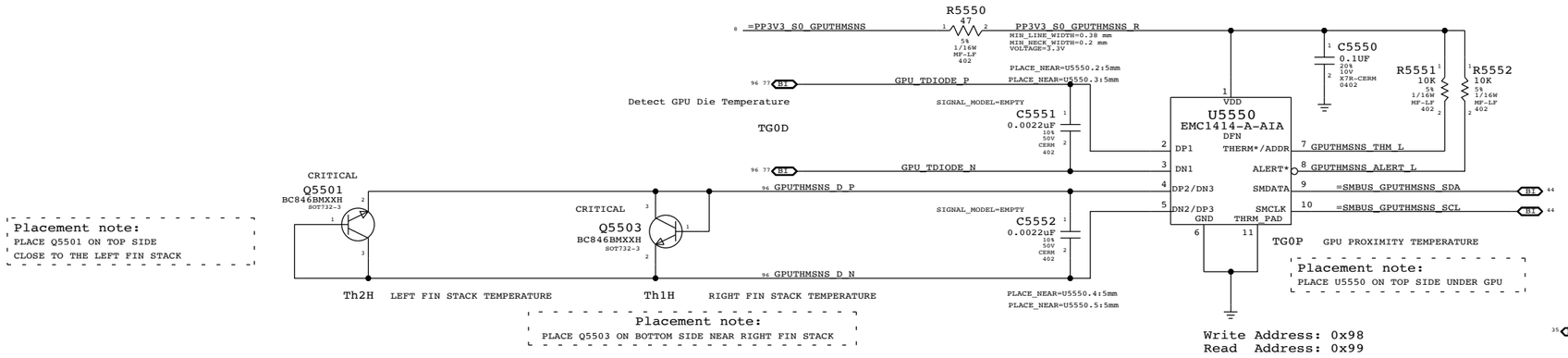
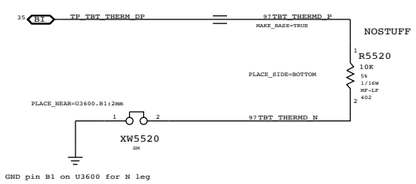
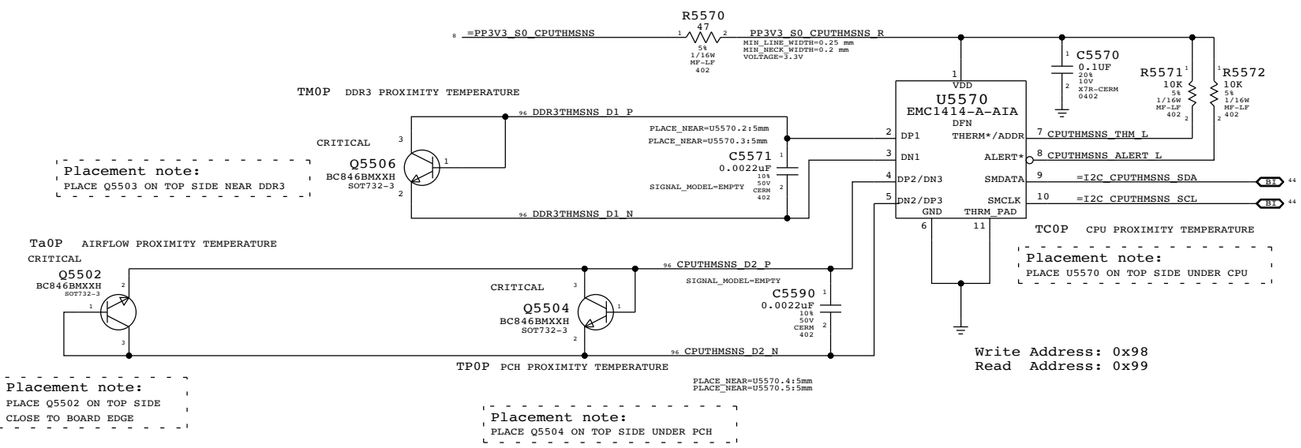
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



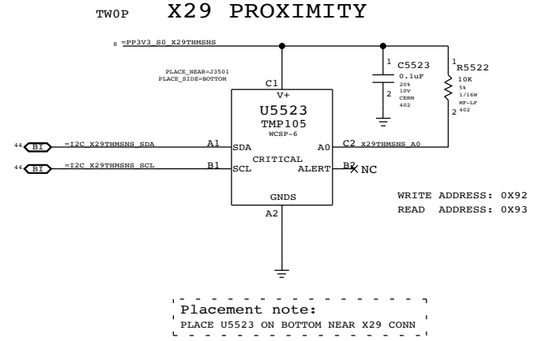
TBT DIE



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X29 PROXIMITY



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Thermal Sensors

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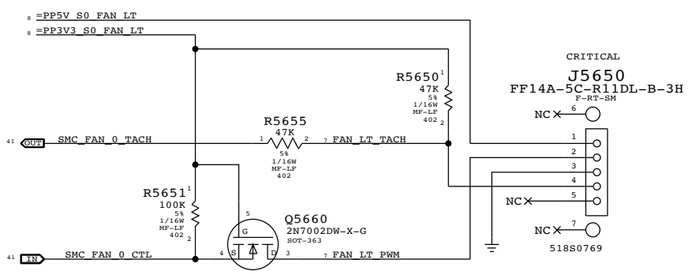
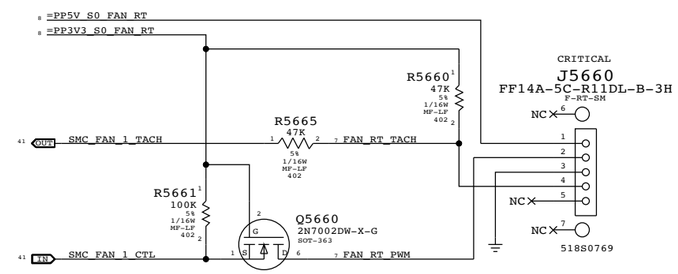
Left Fan



Right Fan



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

Fan Connectors

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DRAWING NUMBER 051-9589 SIZE D

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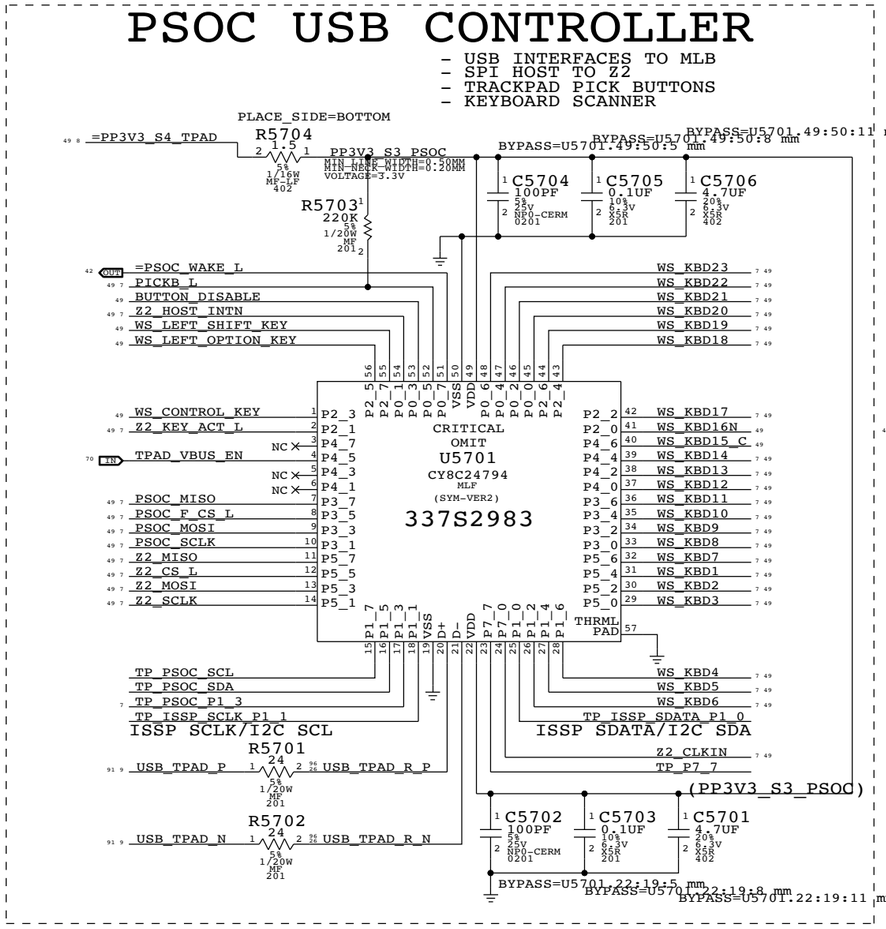
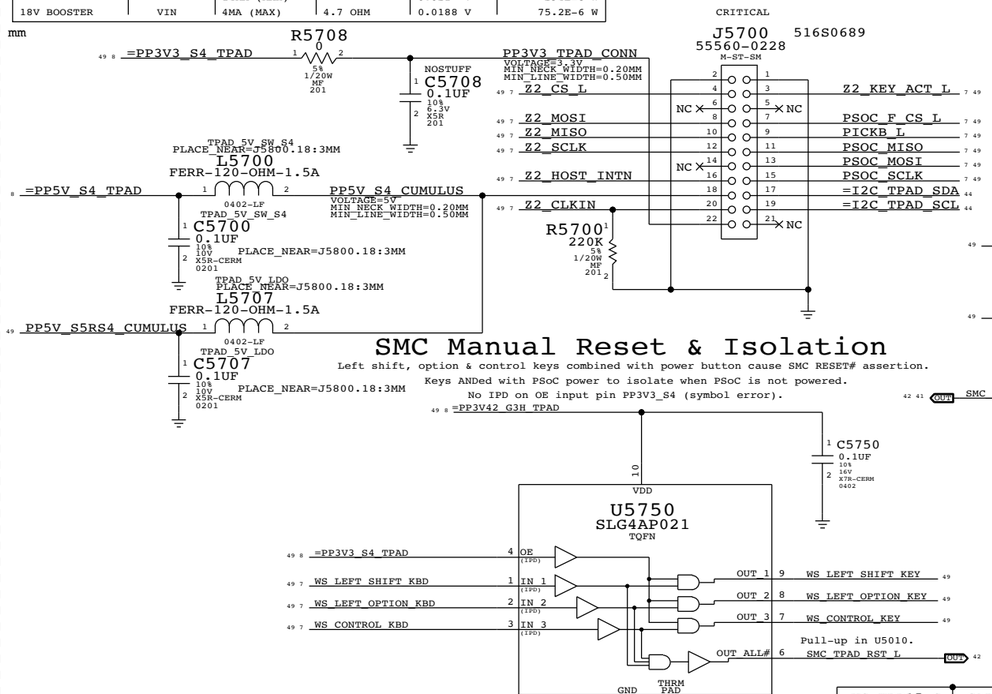
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

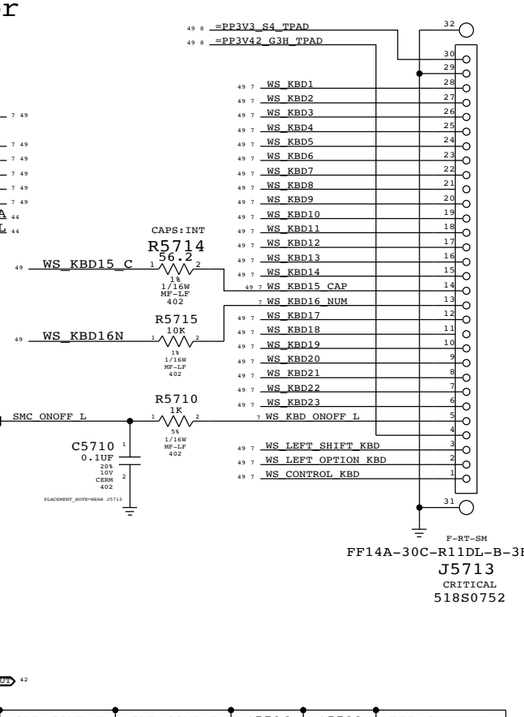


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector



Keyboard Connector

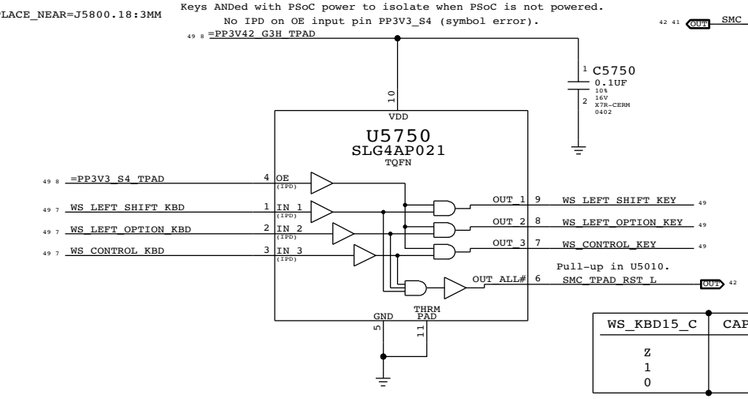


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

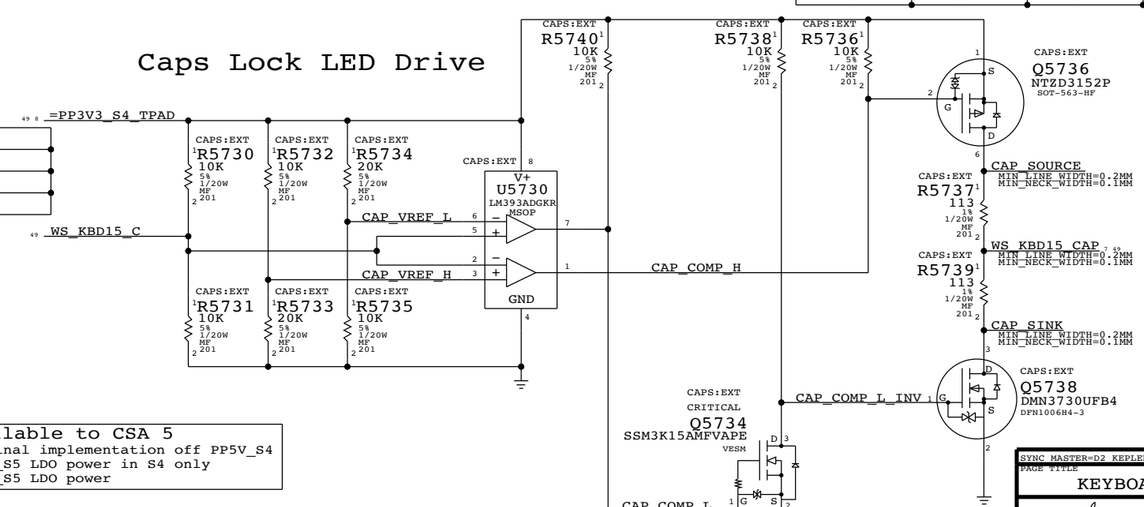
Keys ANDed with PSoC power to isolate when PSoC is not powered.

No IPD on OE input pin PP3V3_S4 (symbol error).



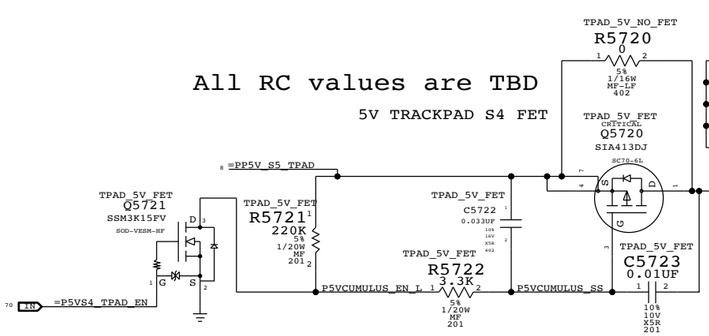
WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

Caps Lock LED Drive



All RC values are TBD

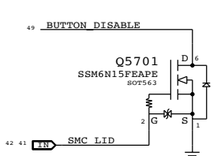
5V TRACKPAD S4 FET



5V TPAD FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800

THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

BOM Options available to CSA 5

TPAD_5V:SW_S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

BOM GROUP	BOM OPTIONS
TPAD_5V:SW_S4	TPAD_5V_SW_S4
TPAD_5V:LDO_S4	TPAD_5V_FET,TPAD_5V_LDO
TPAD_5V:LDO_S5	TPAD_5V_NO_FET,TPAD_5V_LDO

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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PAGE: 57 OF 132

SHEET: 49 OF 99

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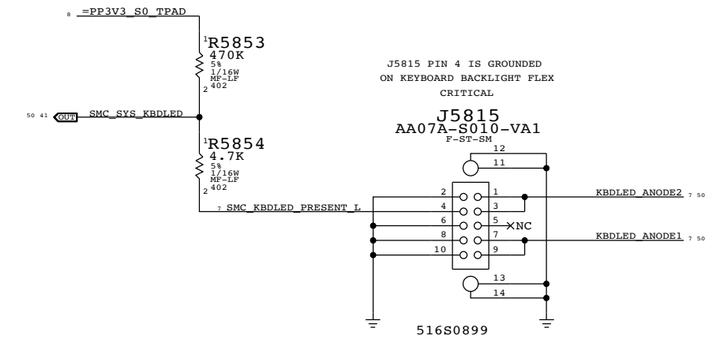
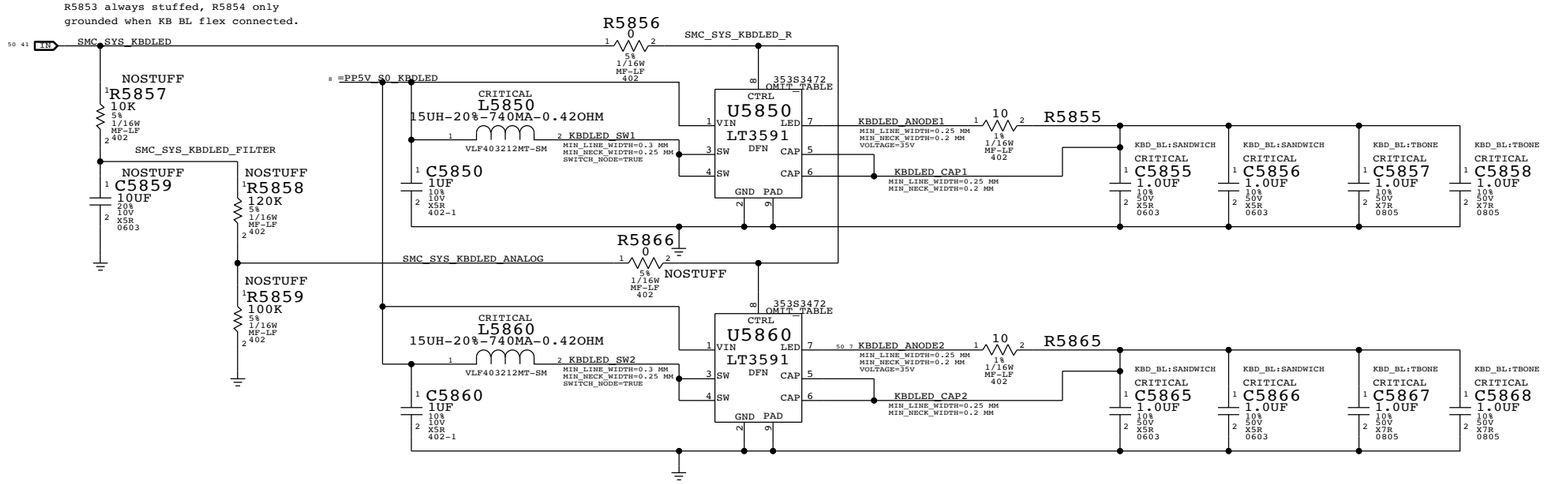


Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will
tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only
grounded when KB BL flex connected.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
35381612	2	IC,DC/DC CVTR,BOOST,WHITE LED,1MHZ,DFN8	U5850,U5860	CRITICAL	

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

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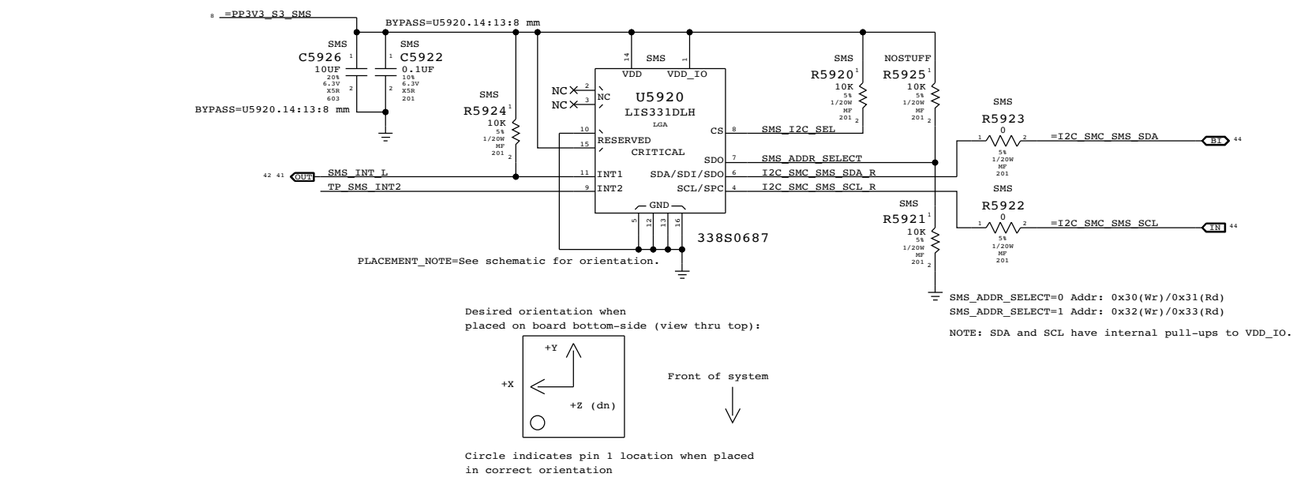


SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

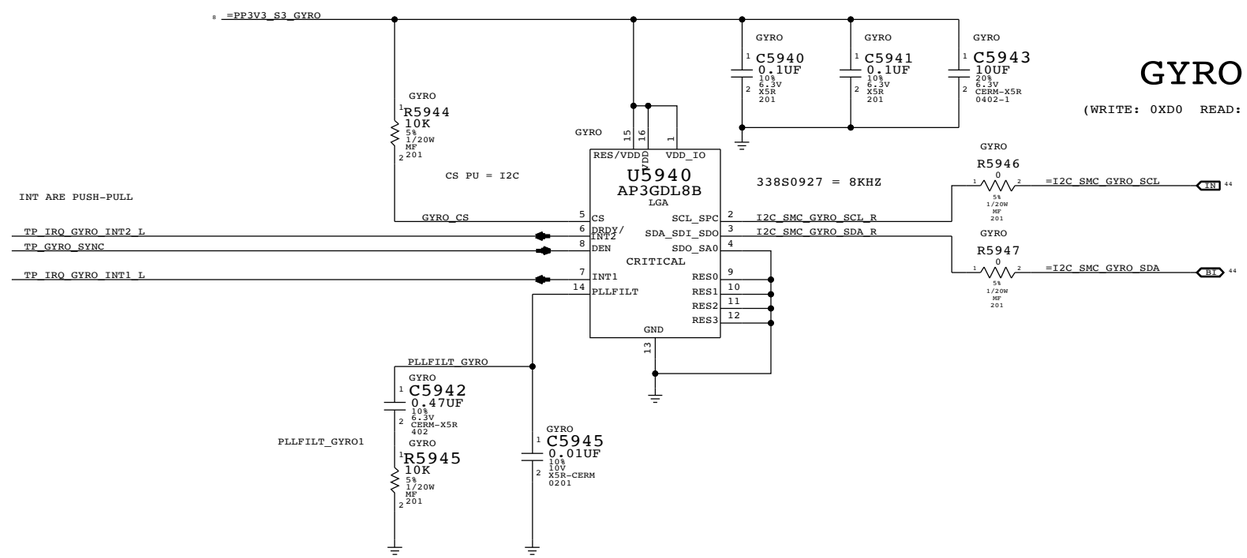
NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when
placed on board bottom-side (view thru top):

Circle indicates pin 1 location when placed
in correct orientation

GYRO

(WRITE: 0XD0 READ: 0XD1)



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
DIGITAL ACCELEROMETER & GYRO

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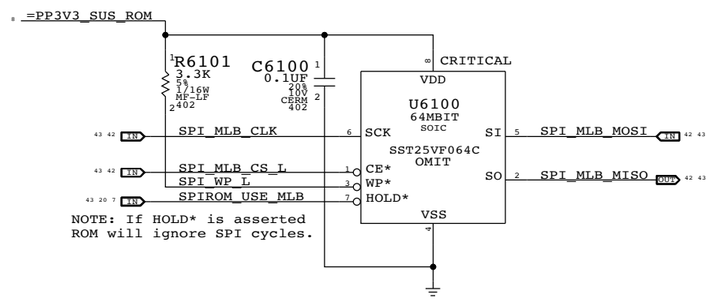

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

SPI ROM

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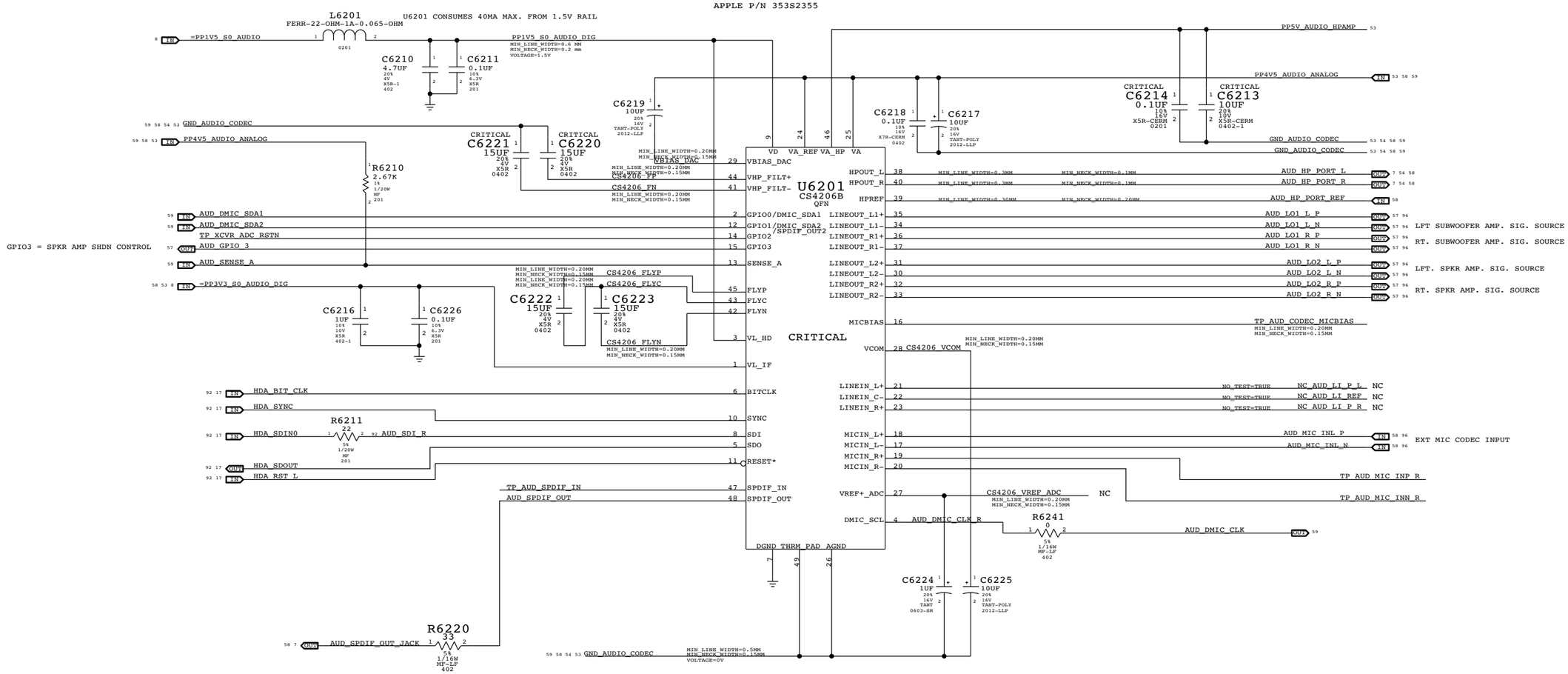
AUDIO CODEC

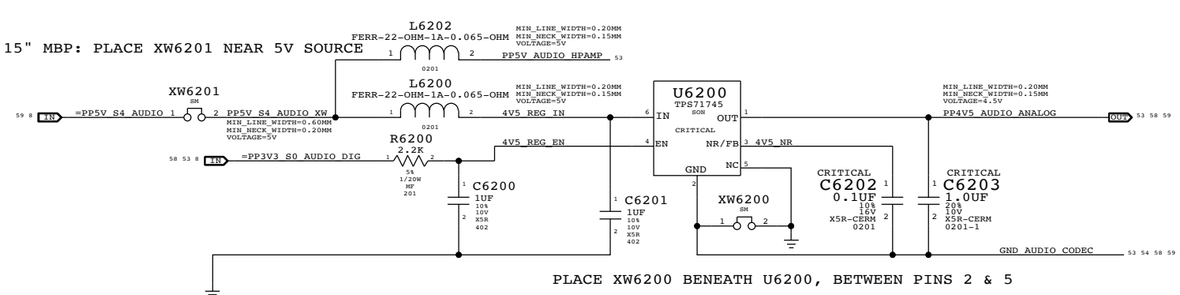
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

15" MBP: PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=D2 CARA SYNC DATE=03/16/2012

PAGE TITLE
AUDIO: CODEC/REGULATOR

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DRAWING NUMBER 051-9589 SIZE D
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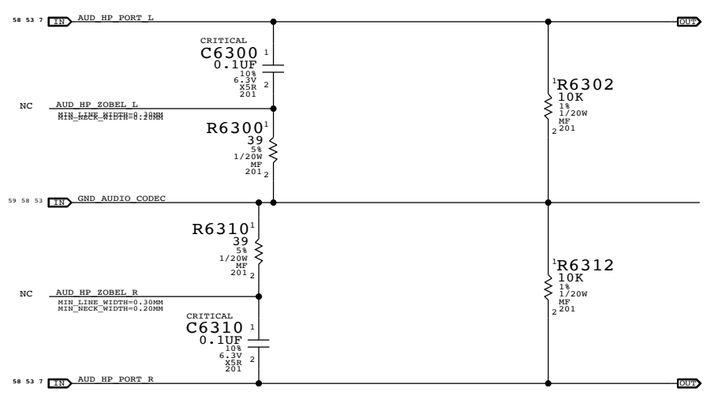
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=D2 CARA SYNC DATE=03/16/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

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PAGE TITLE

AUDIO: IV SENSE

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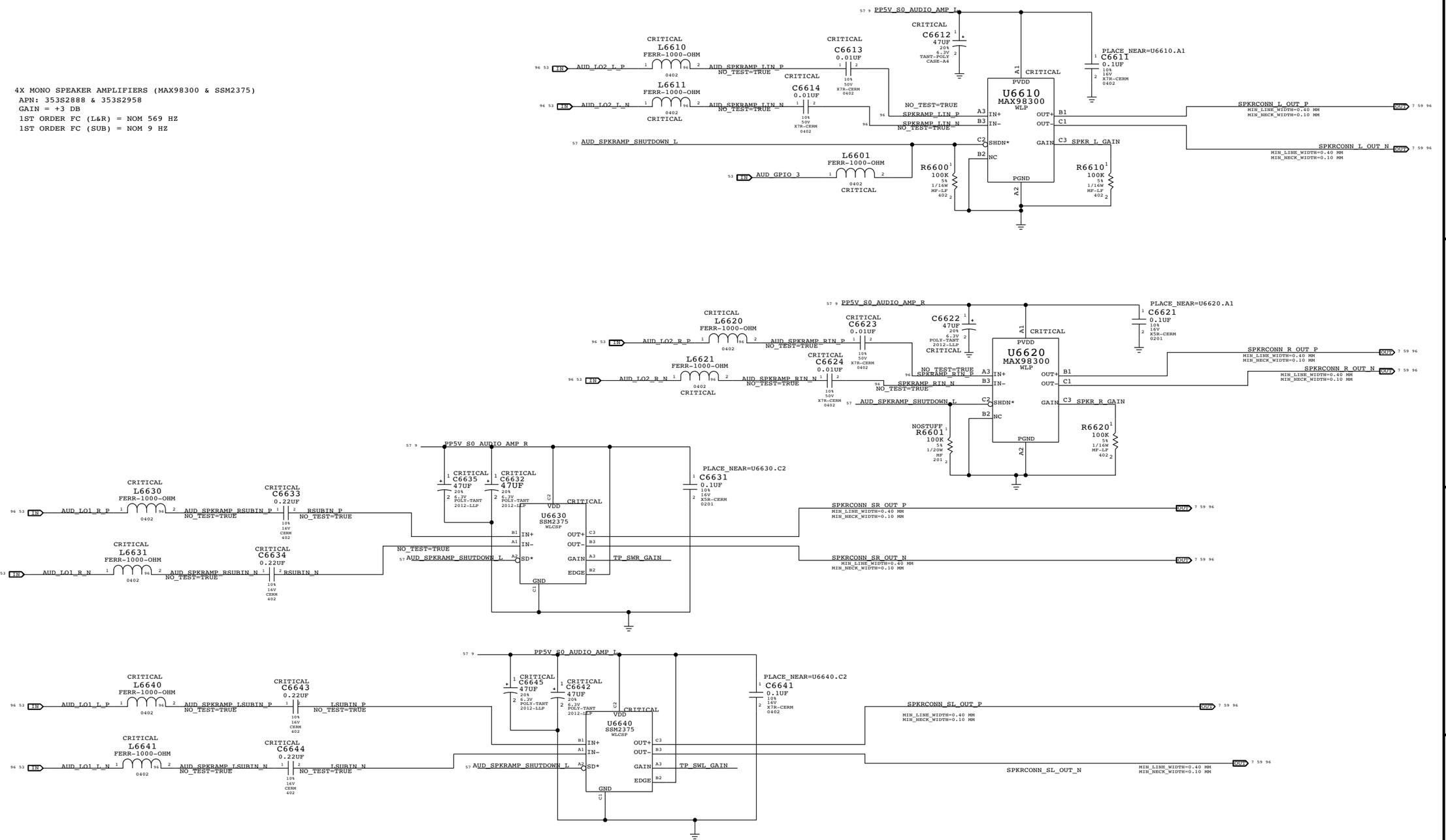
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=D2 CARA SYNC DATE=03/16/2012

PAGE TITLE

AUDIO: SPEAKER AMP

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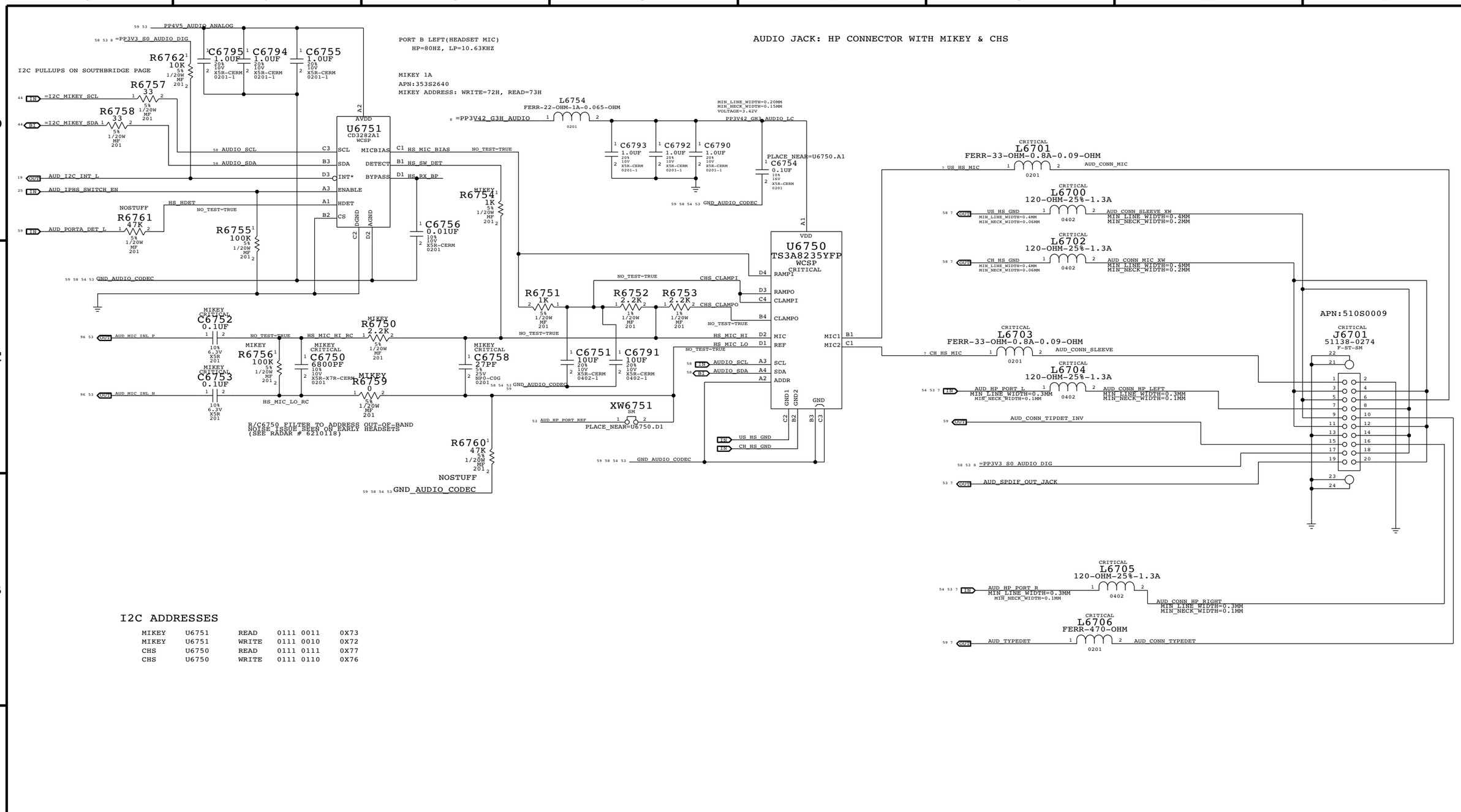

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE: AUDIO: JACK

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DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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CODEC OUTPUT SIGNAL PATHS

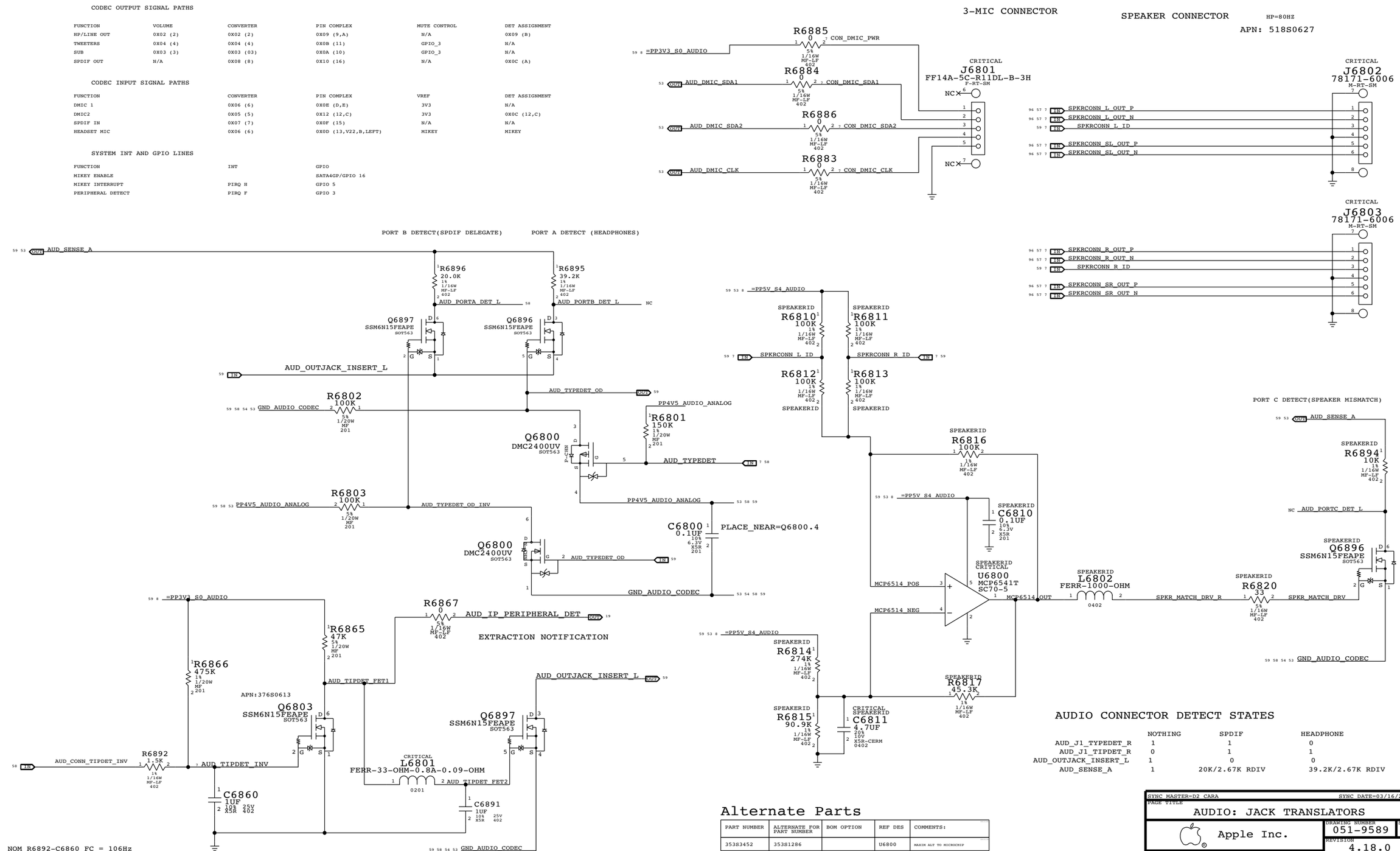
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3



AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353834 52	353812 86		U6800	MAXIM ALT TO MICROCHIP

SYNC MASTER=D2 CARA SYNC DATE=03/16/2012
PAGE TITLE
AUDIO: JACK TRANSLATORS

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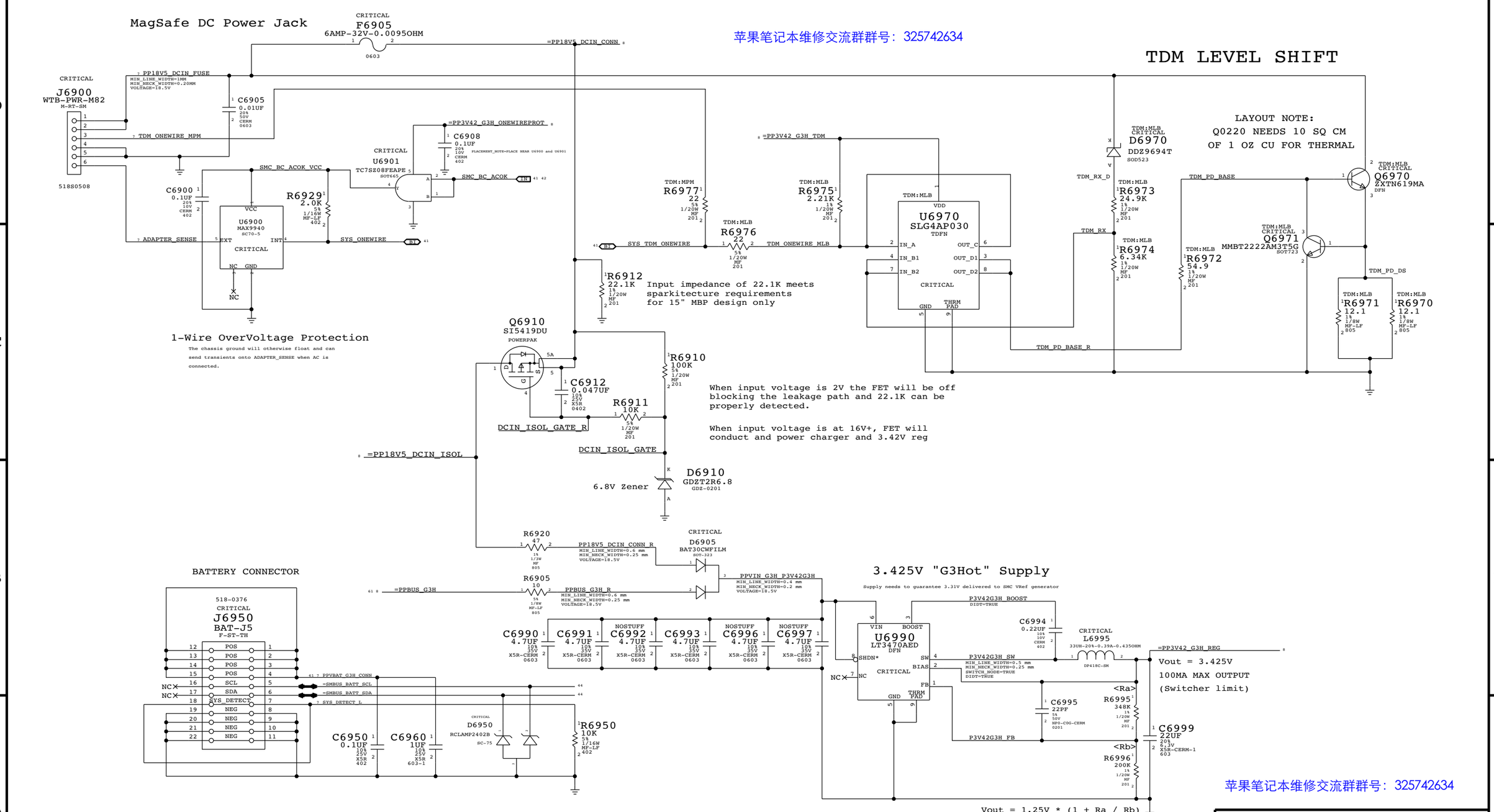

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

DC-In & Battery Connectors

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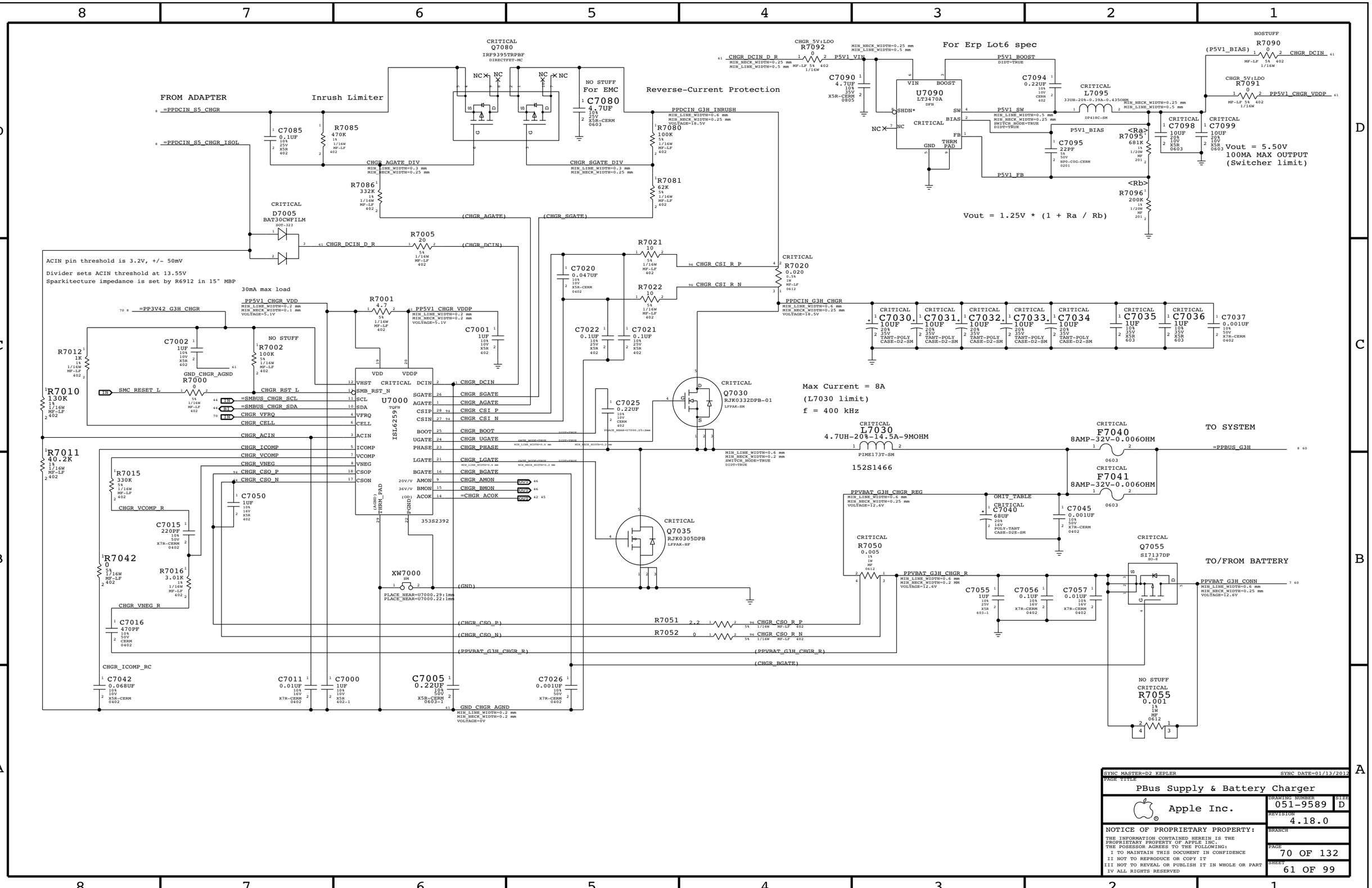

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PAGE TITLE

PBus Supply & Battery Charger

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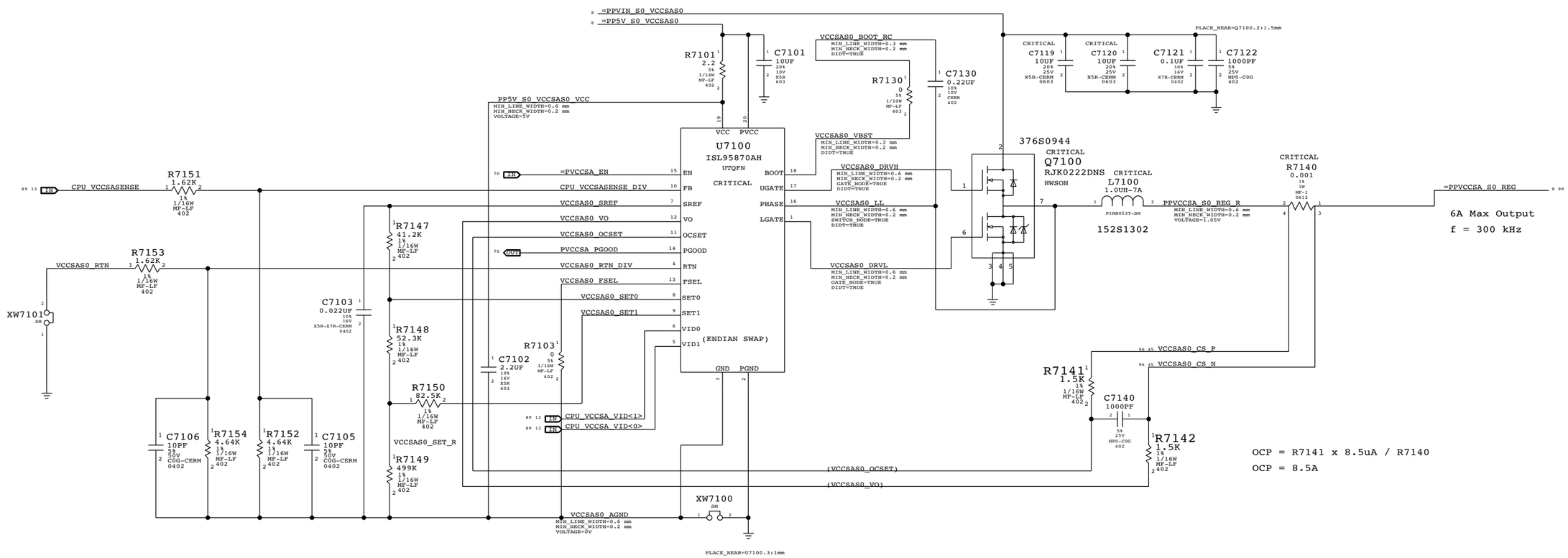

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

fb = (R7151+R7152)/R7152 = 1.349 and Vref = 0.5;

VID1=1, VIC0=1:
Vout<1,1> = Vref x fb;

VID1=0, VID0=1:
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149)) x fb

VID1=1, VID0=0
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149)) x fb

VID1=0, VID0=0
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150)) x fb

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
System Agent Supply

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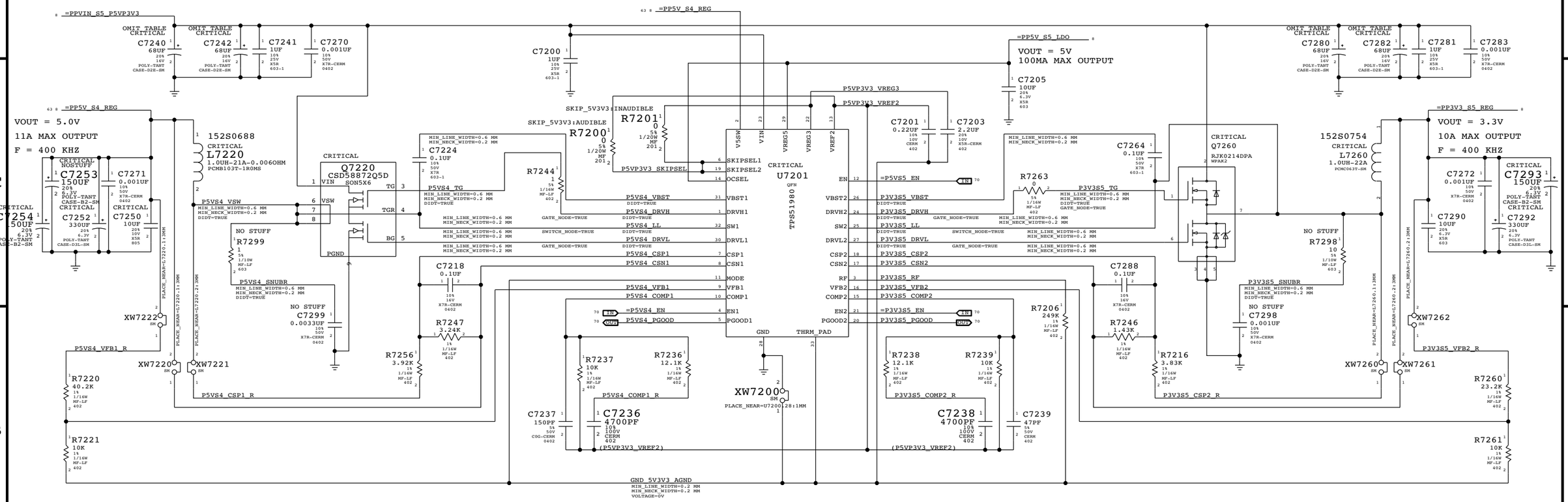

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

5V / 3.3V Power Supply

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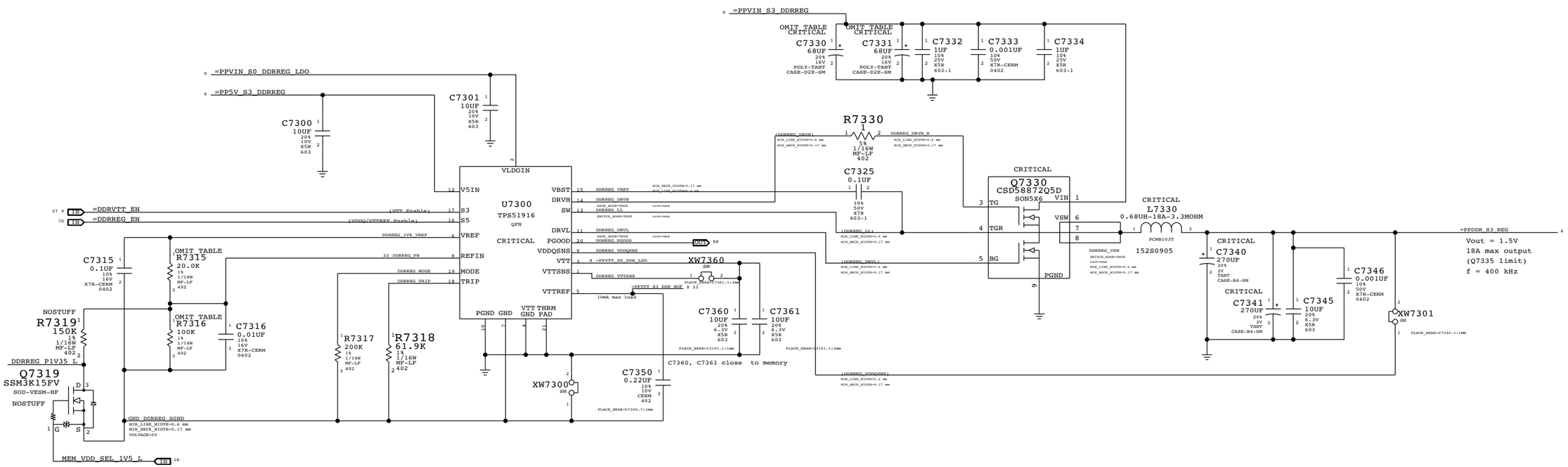
DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R7315		PPDDR:1V5
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7315		PPDDR:1V35
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316		PPDDR:1V5
114S0389	1	RES,MTL FILM,1/16W,57.6K,1,0402,SMD,LF	R7316		PPDDR:1V35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
1V5R1V35V DDR3 SUPPLY

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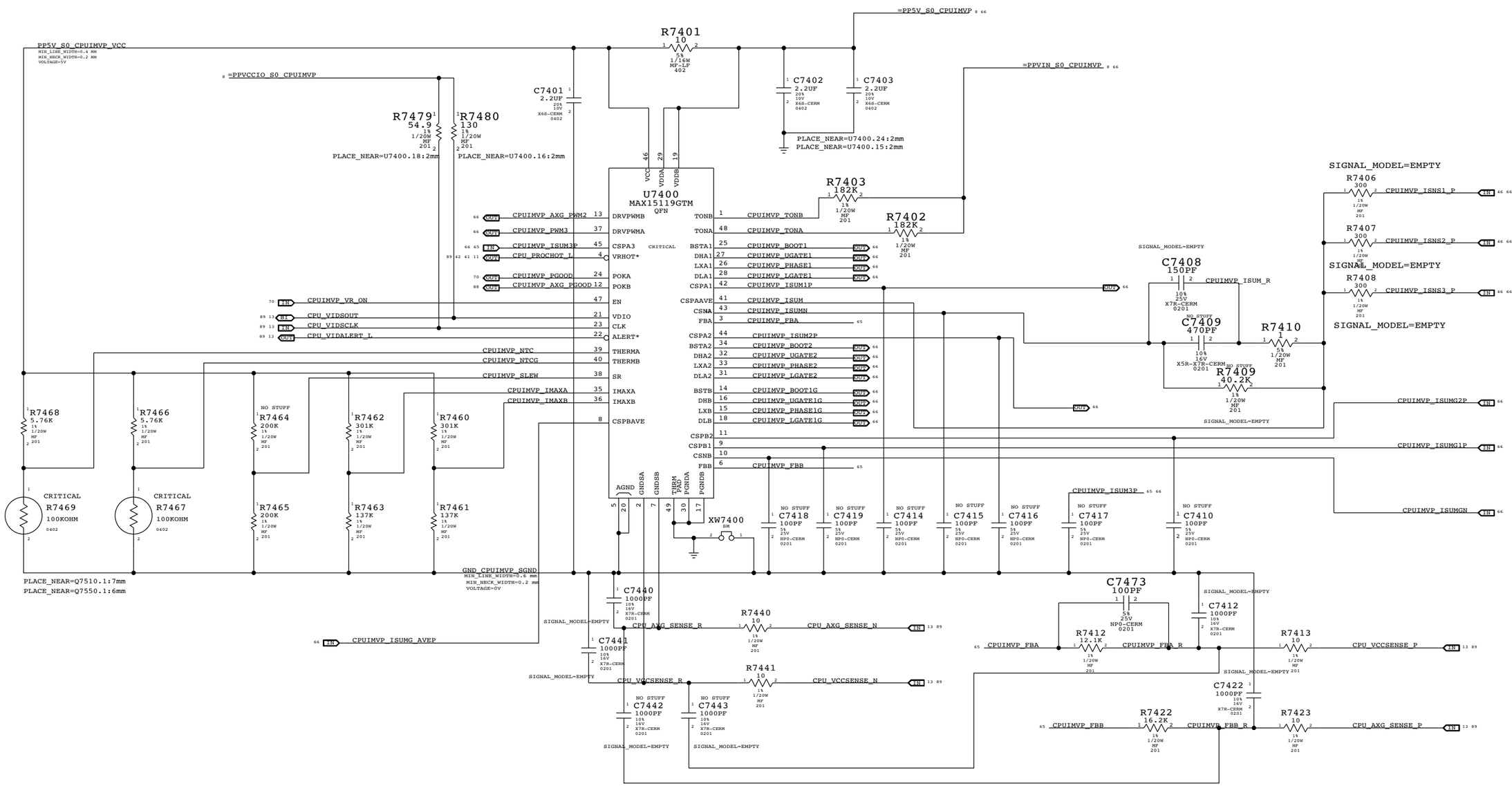

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

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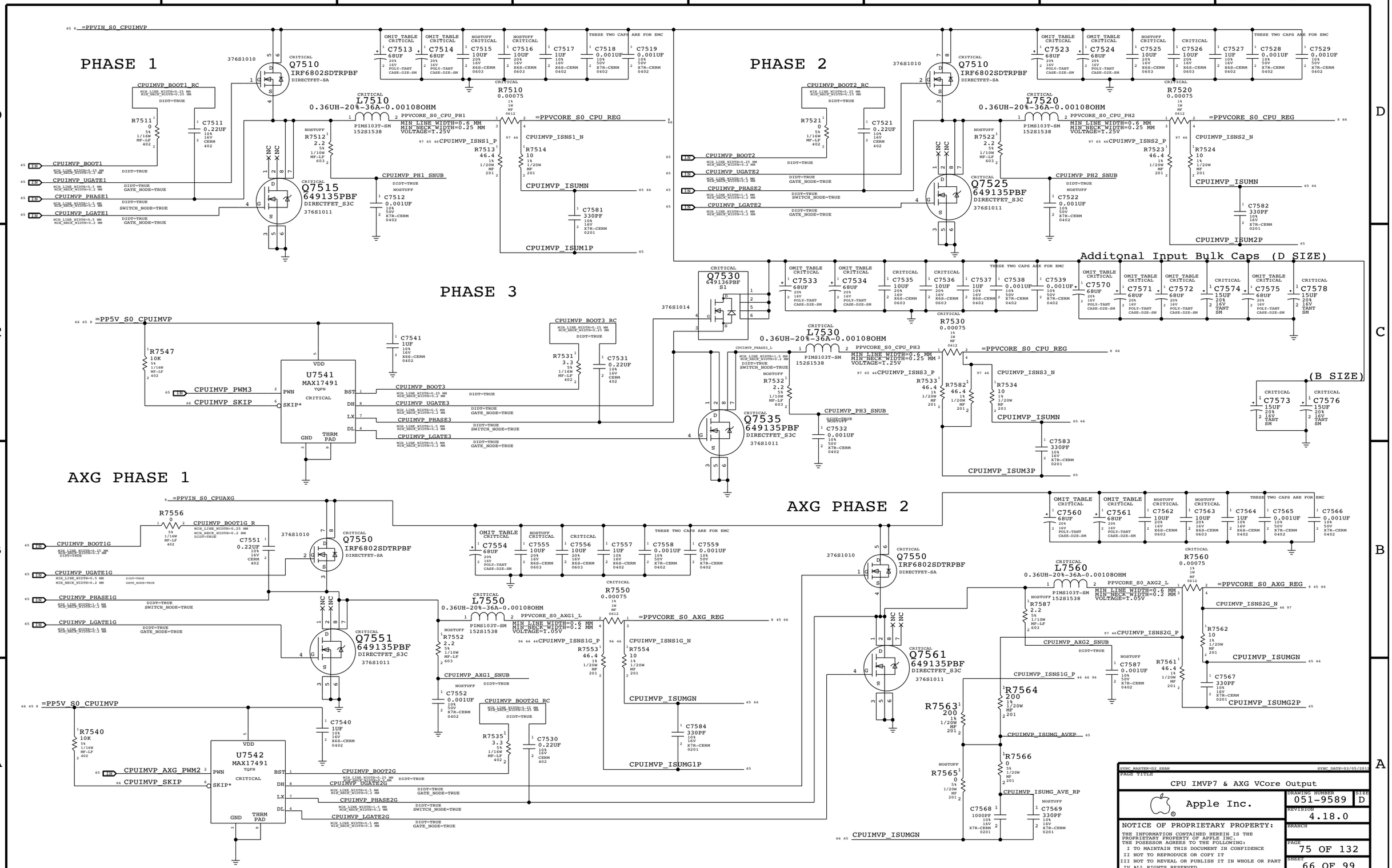
PHASE 1
PHASE 2
PHASE 3
Additonal Input Bulk Caps (D SIZE)
(B SIZE)
AXG PHASE 1
AXG PHASE 2
=PPVIN_S0_CPUIMVP
=PPVCORE_S0_CPU_REG
=PPVCORE_S0_AXG_REG
=PP5V_S0_CPUIMVP
=PPVIN_S0_CPUAXG
Q7510 IRF6802SDTRPBF DIRECTFET-SA
Q7515 649135PBF DIRECTFET_S3C
Q7525 649135PBF DIRECTFET_S3C
Q7530 649136PBF S1
Q7535 649135PBF DIRECTFET_S3C
Q7550 IRF6802SDTRPBF DIRECTFET-SA
Q7551 649135PBF DIRECTFET_S3C
Q7561 649135PBF DIRECTFET_S3C
U7541 MAX17491 TQFN
U7542 MAX17491 TQFN
L7510 0.36UH-20%-36A-0.00108OHM
L7520 0.36UH-20%-36A-0.00108OHM
L7530 0.36UH-20%-36A-0.00108OHM
L7550 0.36UH-20%-36A-0.00108OHM
L7560 0.36UH-20%-36A-0.00108OHM
CPUIMVP_ISUMN
CPUIMVP_ISUM1P
CPUIMVP_ISUM2P
CPUIMVP_ISUM3P
CPUIMVP_ISUMGN
CPUIMVP_ISUMG1P
CPUIMVP_ISUMG2P
CPUIMVP_ISUMG_AVE_RP
CPUIMVP_PWM3
CPUIMVP_SKIP
CPUIMVP_AXG_PWM2
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
CPUIMVP_BOOT3
CPUIMVP_UGATE3
CPUIMVP_PHASE3
CPUIMVP_LGATE3
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
CPUIMVP_BOOT2G
CPUIMVP_UGATE2G
CPUIMVP_PHASE2G
CPUIMVP_LGATE2G
CPU IMVP7 & AXG VCore Output
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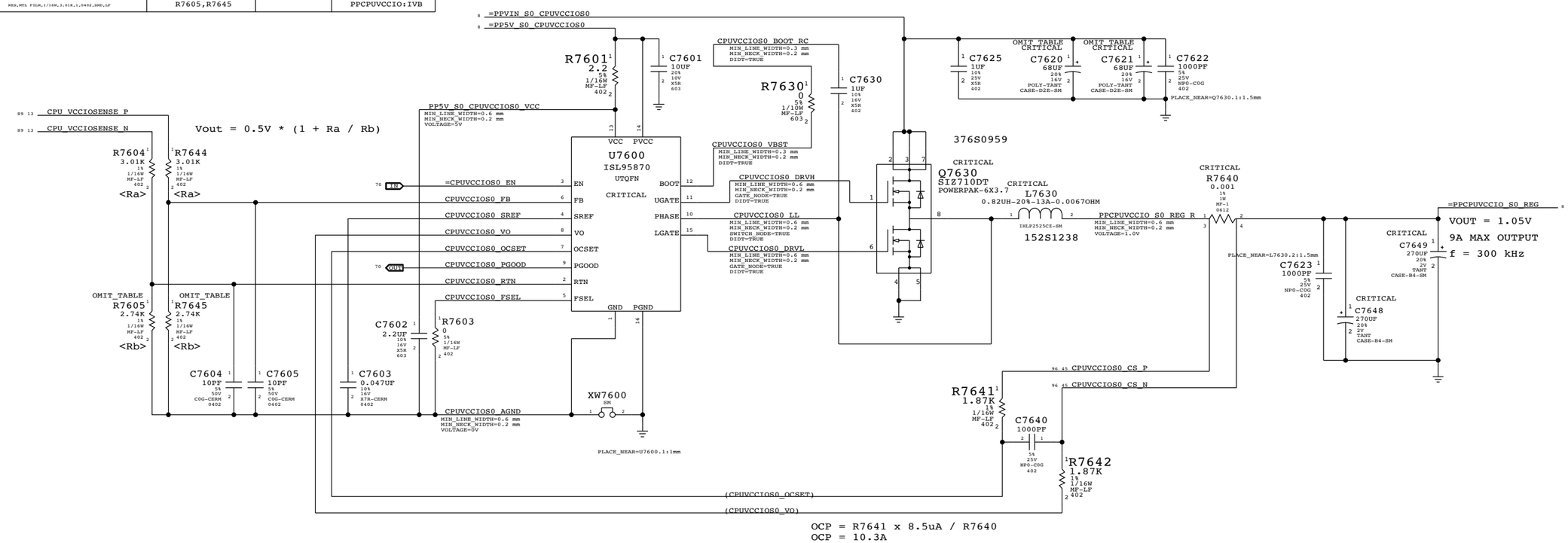
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	RES,MTL FILM,1/16W,2.74K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	RES,MTL FILM,1/16W,3.01K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:IVB



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

CPU VCCIO (1V0R1V05 S0) POWER SUPPLY

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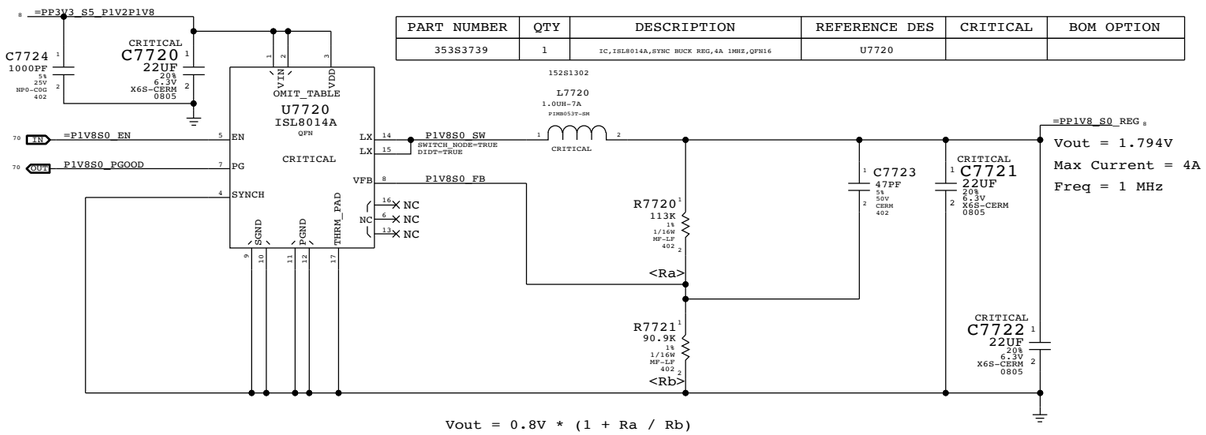
1.8V S0 Regulator

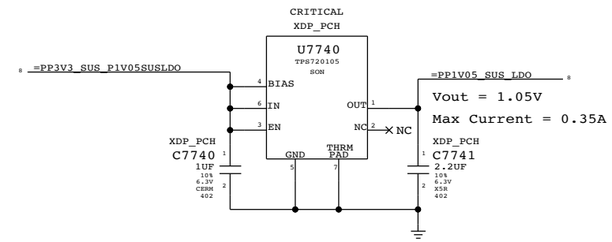
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3739	1	IC,ISL8014A,SYNC BUCK REG,4A 1MHZ,QFN16	U7720		



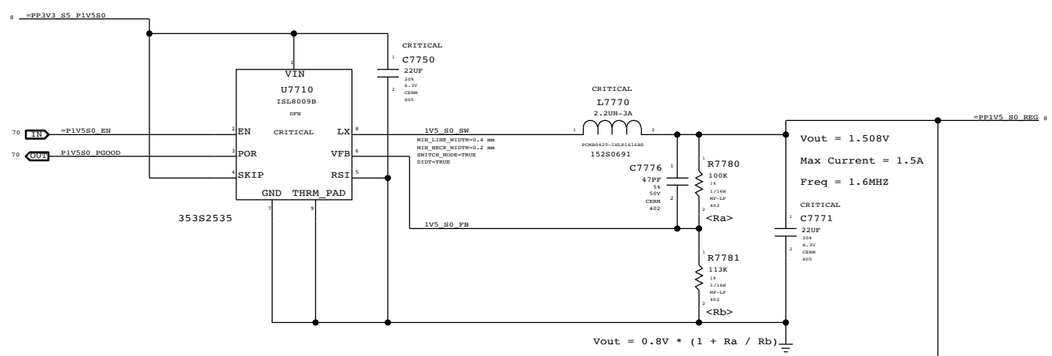
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

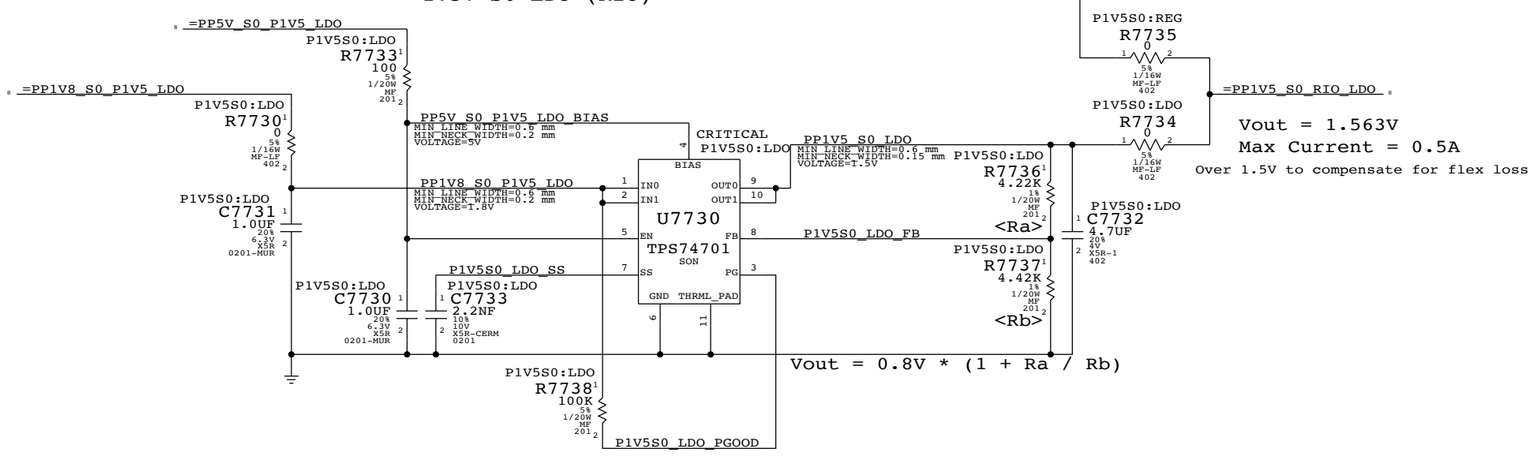
Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



1.5V S0 Regulator



1.5V S0 LDO (RIO)



SYNC MASTER=D2 KEPLER — SYNC DATE=01/13/2012

PAGE TITLE: Misc Power Supplies

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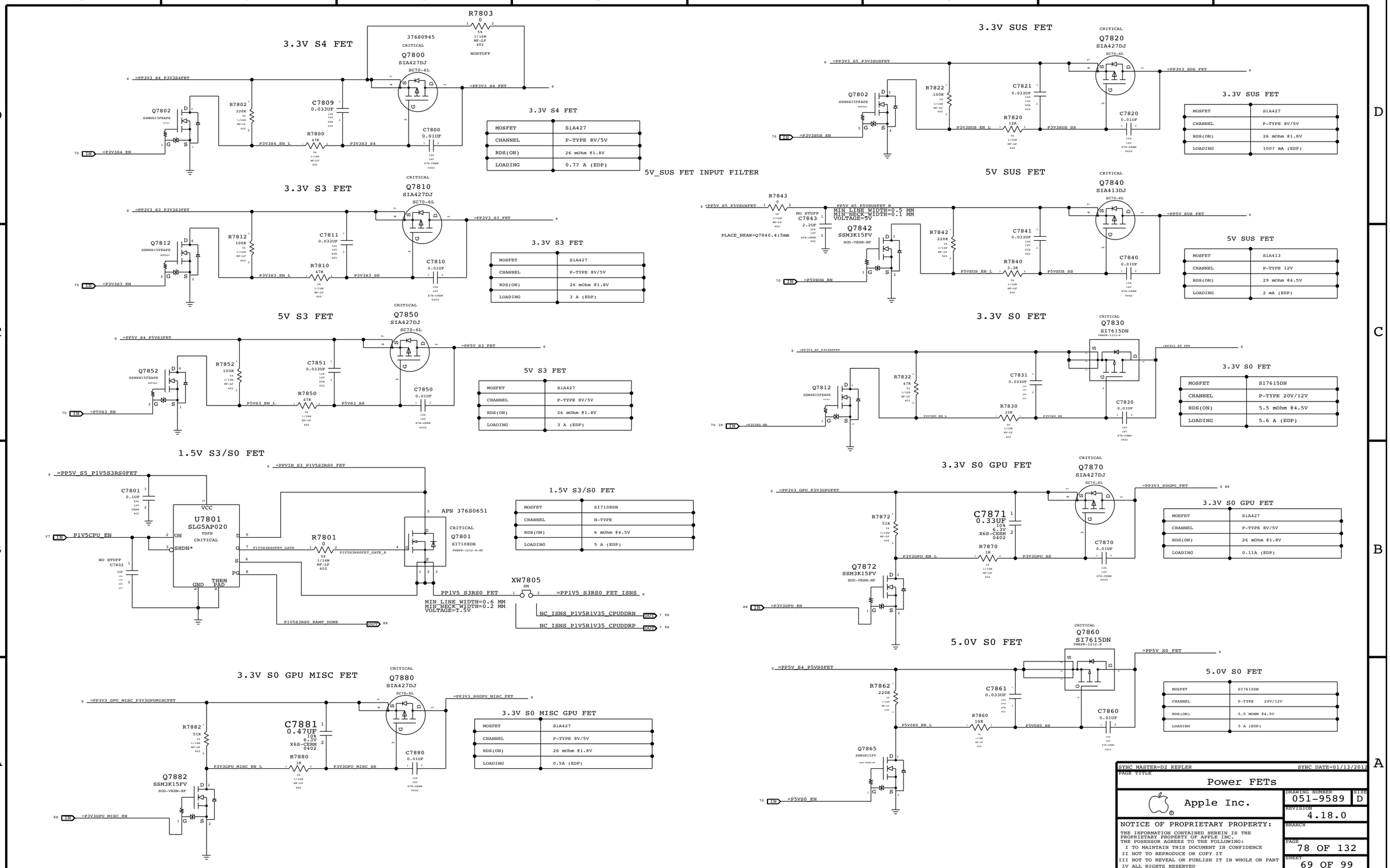
3.3V S4 FET
R7803
0
5%
1/16W
MF-LF
402
NOSTUFF
376S0945
CRITICAL
Q7800
SIA427DJ
SC70-6L
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_FET
Q7802
SSM6N15FEAPE
R7802
220K
C7809
0.033UF
R7800
47K
C7800
0.01UF
=P3V3S4_EN
P3V3S4_EN_L
P3V3S3_S4
3.3V S4 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.77 A (EDP)
3.3V SUS FET
Q7820
SIA427DJ
=PP3V3_S5_P3V3SUSFET
=PP3V3_SUS_FET
Q7802
SSM6N15FEAPE
R7822
100K
C7821
0.033UF
R7820
12K
C7820
0.01UF
=P3V3SUS_EN
P3V3SUS_EN_L
P3V3SUS_SS
3.3V SUS FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 100? mA (EDP)
5V_SUS FET INPUT FILTER
R7843
0
NO STUFF
C7843
2.2UF
=PP5V_S5_P5V8USFET
PP5V_S5_P5V8USFET_R
MIN LINE WIDTH=0.5 MM
MIN NECK WIDTH=0.1 MM
VOLTAGE=5V
PLACE_NEAR=Q7840.4i5mm
Q7842
SSM3K15FV
SOD-VESM-HF
5V SUS FET
Q7840
SIA413DJ
=PP5V_S5_FET
R7842
220K
C7841
0.033UF
R7840
3.3K
C7840
0.01UF
=P5V8US_EN
P5V8US_EN_L
P5V8US_SS
5V SUS FET
MOSFET SiA413
CHANNEL P-TYPE 12V
RDS(ON) 29 mOhm @4.5V
LOADING 2 mA (EDP)
3.3V S3 FET
Q7810
SIA427DJ
=PP3V3_S3_P3V3S3FET
=PP3V3_S3_FET
Q7812
SSM6N15FEAPE
R7812
100K
C7811
0.033UF
R7810
47K
C7810
0.01UF
=P3V3S3_EN
P3V3S3_EN_L
P3V3S3_SS
3.3V S3 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 3 A (EDP)
3.3V S0 FET
Q7830
SI7615DN
=PP3V3_S0_P3V3S0FET
=PP3V3_S0_FET
Q7812
SSM6N15FEAPE
R7832
47K
C7831
0.033UF
R7830
33K
C7830
0.01UF
=P3V3S0_EN
P3V3S0_EN_L
P3V3S0_SS
3.3V S0 FET
MOSFET SI7615DN
CHANNEL P-TYPE 20V/12V
RDS(ON) 5.5 mOhm @4.5V
LOADING 5.6 A (EDP)
5V S3 FET
Q7850
SIA427DJ
=PP5V_S4_P5VS3FET
=PP5V_S3_FET
Q7852
SSM6N15FEAPE
R7852
100K
C7851
0.033UF
R7850
47K
C7850
0.01UF
=P5VS3_EN
P5VS3_EN_L
P5VS3_SS
5V S3 FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 3 A (EDP)
1.5V S3/S0 FET
=PP5V_S5_P1V5S3RS0FET
=PPVIN_S3_P1V5S3RS0_FET
C7801
0.1UF
VCC
U7801
SLG5AP020
TDFN
CRITICAL
ON
SHDN*
GND
THRM PAD
P1V5CPU_EN
NO STUFF
C7802
1UF
R7801
0
5%
1/16W
MF-LF
402
P1V5S3RS0FET_GATE
P1V5S3RS0FET_GATE_R
APN 376S0651
CRITICAL
Q7801
SI7108DN
PWRPK-1212-8-HF
PP1V5_S3RS0_FET
MIN LINE WIDTH=0.6 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.5V
P1V5S3RS0_RAMP_DONE
XW7805
SM
=PP1V5_S3RS0_FET_ISNS
NC_ISNS_P1V5R1V35_CPUDDRN
NC_ISNS_P1V5R1V35_CPUDDRP
1.5V S3/S0 FET
MOSFET SI7108DN
CHANNEL N-TYPE
RDS(ON) 6 mOhm @4.5V
LOADING 5 A (EDP)
3.3V S0 GPU FET
Q7870
SIA427DJ
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S0GPU_FET
R7872
51K
C7871
0.33UF
10%
6.3V
X6S-CERM
0402
R7870
1K
C7870
0.01UF
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P3V3GPU_SS
Q7872
SSM3K15FV
SOD-VESM-HF
=P3V3GPU_EN
3.3V S0 GPU FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.11A (EDP)
3.3V S0 GPU MISC FET
Q7880
SIA427DJ
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=PP3V3_S0GPU_MISC_FET
R7882
51K
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10%
6.3V
X6S-CERM
0402
R7880
1K
C7880
0.01UF
P3V3GPU_MISC_EN_L
P3V3GPU_MISC_SS
Q7882
SSM3K15FV
SOD-VESM-HF
=P3V3GPU_MISC_EN
3.3V S0 MISC GPU FET
MOSFET SiA427
CHANNEL P-TYPE 8V/5V
RDS(ON) 26 mOhm @1.8V
LOADING 0.5A (EDP)
5.0V S0 FET
Q7860
SI7615DN
PWRPK-1212-8
=PP5V_S0_FET
=PP5V_S4_P5VS0FET
R7862
220K
C7861
0.033UF
R7860
10K
C7860
0.01UF
P5VS0_EN_L
P5VS0_SS
Q7865
SSM3K15FV
SOD-VESM-HF
=P5VS0_EN
5.0V S0 FET
MOSFET SI7615DN
CHANNEL P-TYPE 20V/12V
RDS(ON) 5.5 MOHM @4.5V
LOADING 5 A (EDP)
SYNC MASTER=D2 KEPLER
SYNC DATE=01/13/2013
PAGE TITLE
Power FETs
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
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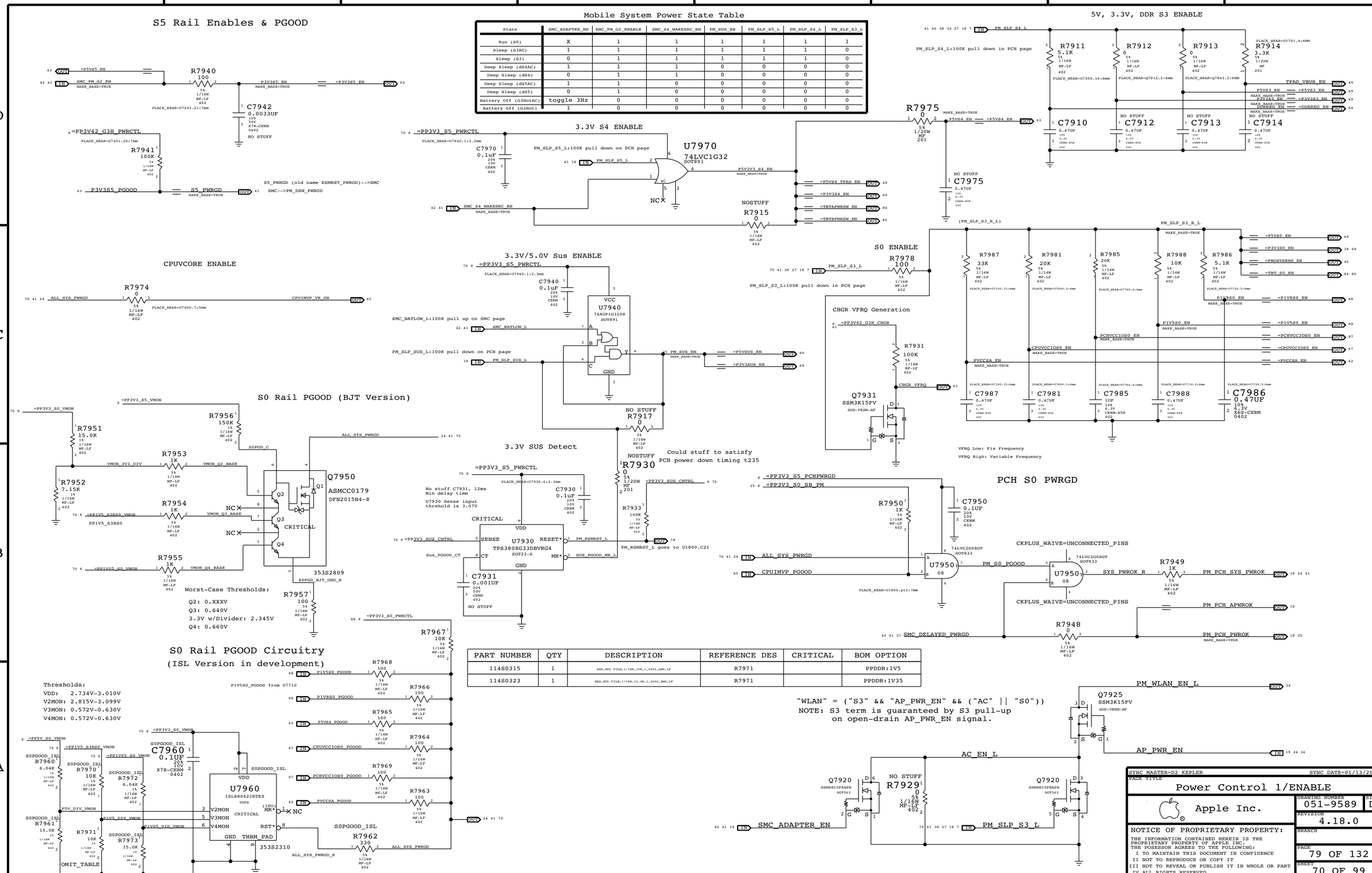

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES,MTL FILM,1/16W,10K,1,0402,SMD,LF	R7971		PPDDR:1V5
114S0323	1	RES,MTL FILM,1/16W,12.4K,1,0402,SMD,LF	R7971		PPDDR:1V35

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

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89 9	IN	PEG_R2D_C_P<1>	C8022	0.22UF	GND_VOID=TRUE	PEG_R2D_P<1>	71 89
89 9	IN	PEG_R2D_C_N<1>	C8023	0.22UF	GND_VOID=TRUE	PEG_R2D_N<1>	71 89
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89 9	IN	PEG_R2D_C_N<2>	C8025	0.22UF	GND_VOID=TRUE	PEG_R2D_N<2>	71 89
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89 71	PEG_D2R_C_P<1>	C8057	0.22UF	GND_VOID=TRUE	PEG_D2R_P<1>	OUT	9 89
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89 71	PEG_D2R_C_N<2>	C8060	0.22UF	GND_VOID=TRUE	PEG_D2R_N<2>	OUT	9 89
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89 71	PEG_D2R_C_P<4>	C8063	0.22UF	GND_VOID=TRUE	PEG_D2R_P<4>	OUT	9 88 89
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89 71	PEG_D2R_C_N<6>	C8068	0.22UF	GND_VOID=TRUE	PEG_D2R_N<6>	OUT	9 89
89 71	PEG_D2R_C_P<7>	C8069	0.22UF	GND_VOID=TRUE	PEG_D2R_P<7>	OUT	9 88 89
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OMIT_TABLE

U8000
NV-GK107
BGA
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78 9	IN GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	
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NC		AJ11	PEX_WAKE*	PEX_SVDD_3V3	AG12	PP3V3_GPU_PEX_PLL_HVDD 79

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R8001: 10K, 1% 1/20W MF 201 — =PP3V3_GPU_VDD33 79 78 77 8 — PEX_CLKREQ_L_R 78 71

NOSTUFF R8002: 200, 1% 1/20W MF 201

R8005: 2.49K, 1% 1/20W MF 201 — GPU_PEX_TERMP

SYNC MASTER=D2 KEPLER — SYNC DATE=01/13/2012

PAGE TITLE: KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-9589 — SIZE: D

REVISION: 4.18.0

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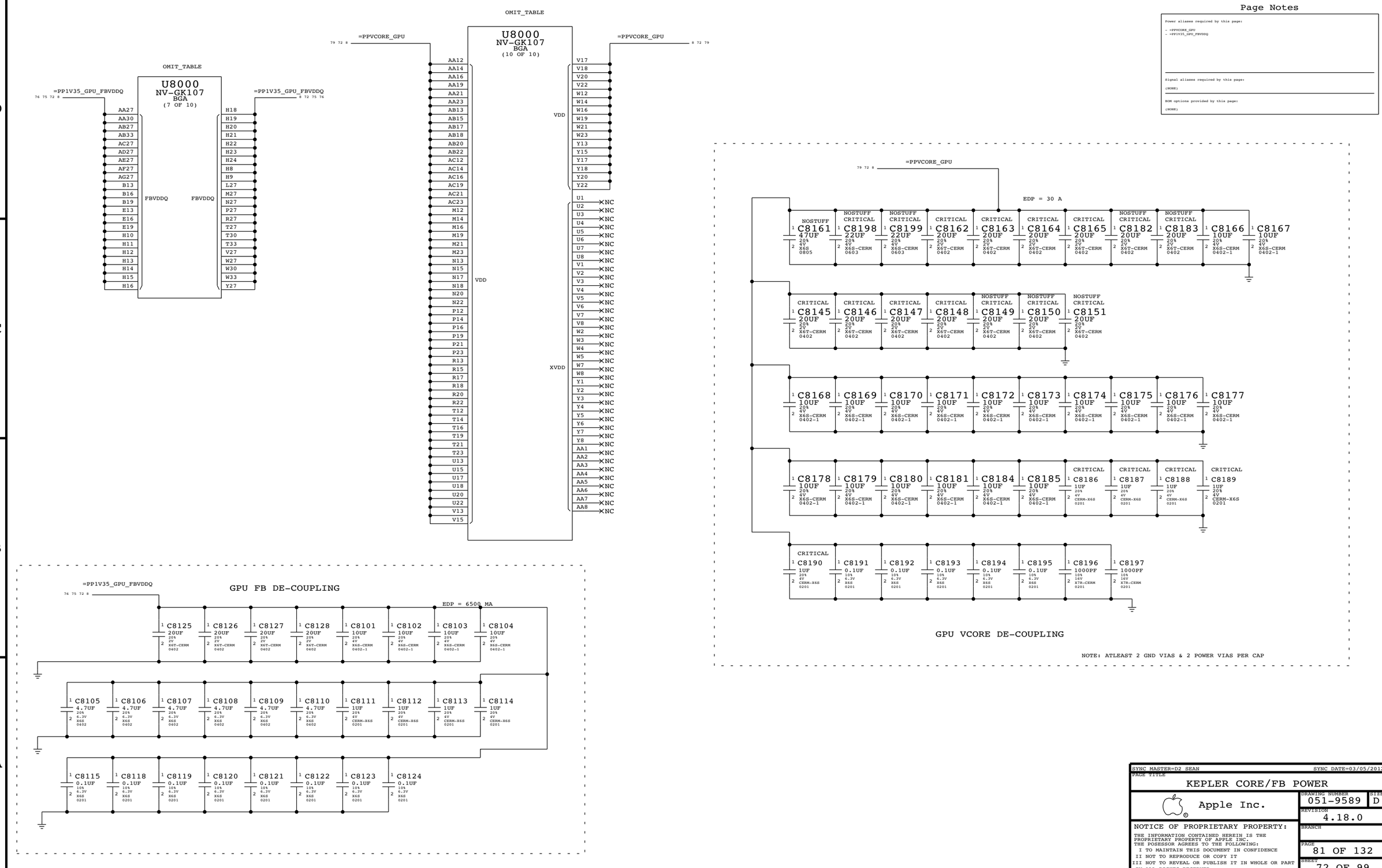

SYNC MASTER=D2 SEAN SYNC DATE=03/05/2013

PAGE TITLE

KEPLER CORE/FB POWER

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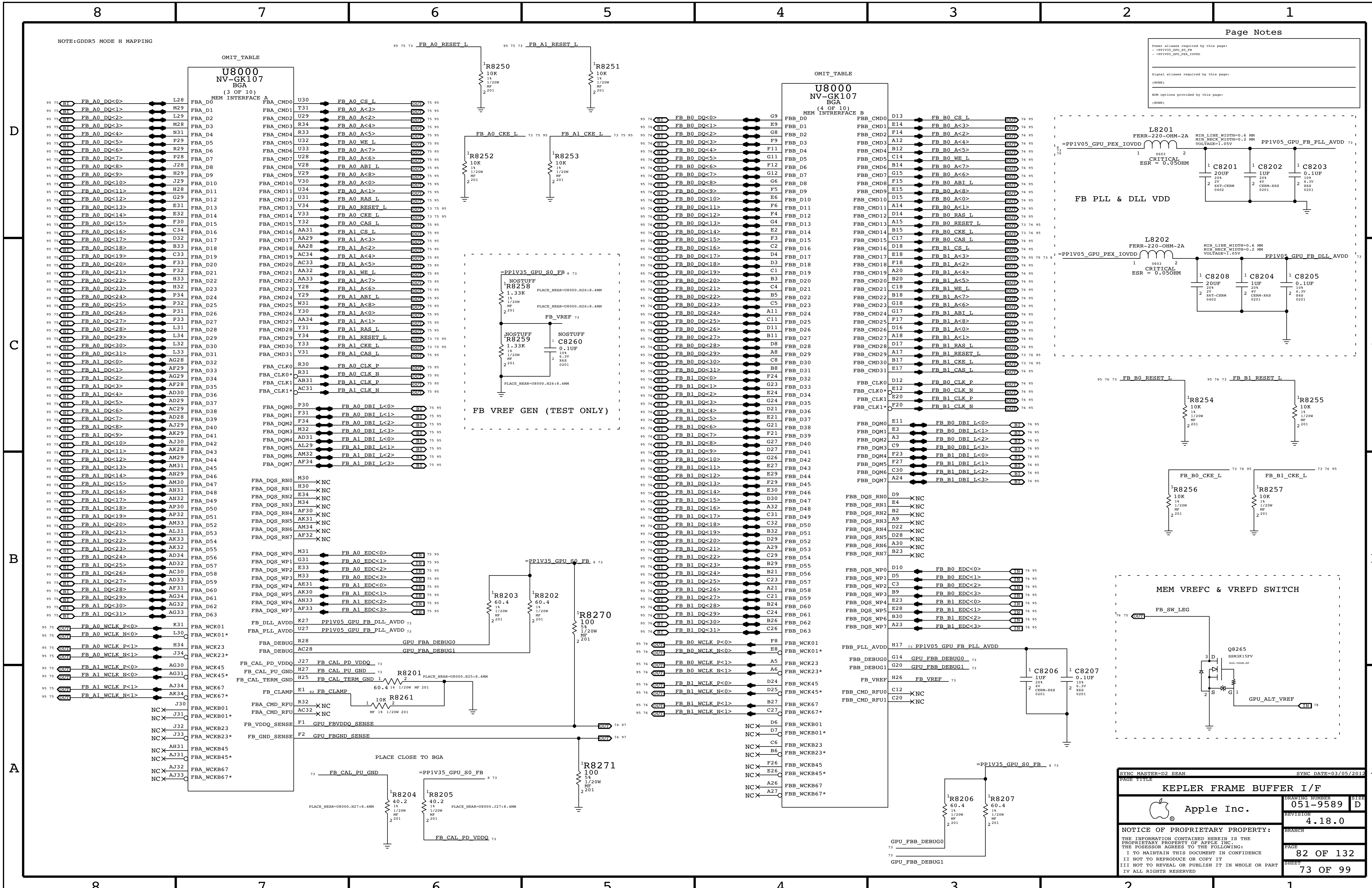
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U8000
NV-GK107
BGA
(3 OF 10)
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R8203 60.4 1% 1/20W MF 201
R8202 60.4 1% 1/20W MF 201
R8270 100 5% 1/20W MF 201
R8271 100 5% 1/20W MF 201
PLACE CLOSE TO BGA
FB_CAL_PU_GND
R8204 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.H27:8.4MM
=PP1V35_GPU_S0_FB
R8205 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.J27:8.4MM
FB_CAL_PD_VDDQ
FB_A0_RESET_L R8250 10K 1% 1/20W MF 201
FB_A1_RESET_L R8251 10K 1% 1/20W MF 201
FB_A0_CKE_L R8252 10K 1% 1/20W MF 201
FB_A1_CKE_L R8253 10K 1% 1/20W MF 201
=PP1V35_GPU_S0_FB
NOSTUFF R8258 1.33K 1% 1/20W MF 201
PLACE_NEAR=U8000.H26:8.4MM
PLACE_NEAR=U8000.H26:8.4MM
FB_VREF
NOSTUFF R8259 1.33K 1% 1/20W MF 201
NOSTUFF C8260 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=U8000.H26:8.4MM
FB VREF GEN (TEST ONLY)
OMIT_TABLE
U8000
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B
FB_B0_DQ<0> G9 FBB_D0
FB_B0_DQ<1> E9 FBB_D1
FB_B0_DQ<2> G8 FBB_D2
FB_B0_DQ<3> F9 FBB_D3
FB_B0_DQ<4> F11 FBB_D4
FB_B0_DQ<5> G11 FBB_D5
FB_B0_DQ<6> F12 FBB_D6
FB_B0_DQ<7> G12 FBB_D7
FB_B0_DQ<8> G6 FBB_D8
FB_B0_DQ<9> F5 FBB_D9
FB_B0_DQ<10> E6 FBB_D10
FB_B0_DQ<11> F6 FBB_D11
FB_B0_DQ<12> F4 FBB_D12
FB_B0_DQ<13> G4 FBB_D13
FB_B0_DQ<14> E2 FBB_D14
FB_B0_DQ<15> F3 FBB_D15
FB_B0_DQ<16> C2 FBB_D16
FB_B0_DQ<17> D4 FBB_D17
FB_B0_DQ<18> D3 FBB_D18
FB_B0_DQ<19> C1 FBB_D19
FB_B0_DQ<20> B3 FBB_D20
FB_B0_DQ<21> C4 FBB_D21
FB_B0_DQ<22> B5 FBB_D22
FB_B0_DQ<23> C5 FBB_D23
FB_B0_DQ<24> A11 FBB_D24
FB_B0_DQ<25> C11 FBB_D25
FB_B0_DQ<26> D11 FBB_D26
FB_B0_DQ<27> B11 FBB_D27
FB_B0_DQ<28> D8 FBB_D28
FB_B0_DQ<29> A8 FBB_D29
FB_B0_DQ<30> C8 FBB_D30
FB_B0_DQ<31> B8 FBB_D31
FB_B1_DQ<0> F24 FBB_D32
FB_B1_DQ<1> G23 FBB_D33
FB_B1_DQ<2> E24 FBB_D34
FB_B1_DQ<3> G24 FBB_D35
FB_B1_DQ<4> D21 FBB_D36
FB_B1_DQ<5> E21 FBB_D37
FB_B1_DQ<6> G21 FBB_D38
FB_B1_DQ<7> F21 FBB_D39
FB_B1_DQ<8> G27 FBB_D40
FB_B1_DQ<9> D27 FBB_D41
FB_B1_DQ<10> G26 FBB_D42
FB_B1_DQ<11> E27 FBB_D43
FB_B1_DQ<12> E29 FBB_D44
FB_B1_DQ<13> F29 FBB_D45
FB_B1_DQ<14> E30 FBB_D46
FB_B1_DQ<15> D30 FBB_D47
FB_B1_DQ<16> A32 FBB_D48
FB_B1_DQ<17> C31 FBB_D49
FB_B1_DQ<18> C32 FBB_D50
FB_B1_DQ<19> B32 FBB_D51
FB_B1_DQ<20> D29 FBB_D52
FB_B1_DQ<21> A29 FBB_D53
FB_B1_DQ<22> C29 FBB_D54
FB_B1_DQ<23> B29 FBB_D55
FB_B1_DQ<24> B21 FBB_D56
FB_B1_DQ<25> C23 FBB_D57
FB_B1_DQ<26> A21 FBB_D58
FB_B1_DQ<27> C21 FBB_D59
FB_B1_DQ<28> B24 FBB_D60
FB_B1_DQ<29> C24 FBB_D61
FB_B1_DQ<30> B26 FBB_D62
FB_B1_DQ<31> C26 FBB_D63
FB_B0_WCLK_P<0> F8 FBB_WCK01
FB_B0_WCLK_N<0> E8 FBB_WCK01*
FB_B0_WCLK_P<1> A5 FBB_WCK23
FB_B0_WCLK_N<1> A6 FBB_WCK23*
FB_B1_WCLK_P<0> D24 FBB_WCK45
FB_B1_WCLK_N<0> D25 FBB_WCK45*
FB_B1_WCLK_P<1> B27 FBB_WCK67
FB_B1_WCLK_N<1> C27 FBB_WCK67*
NC D6 FBB_WCKB01
NC D7 FBB_WCKB01*
NC C6 FBB_WCKB23
NC B6 FBB_WCKB23*
NC F26 FBB_WCKB45
NC E26 FBB_WCKB45*
NC A26 FBB_WCKB67
NC A27 FBB_WCKB67*
FBB_CMD0 D13 FB_B0_CS_L
FBB_CMD1 E14 FB_B0_A<3>
FBB_CMD2 F14 FB_B0_A<2>
FBB_CMD3 A12 FB_B0_A<4>
FBB_CMD4 B12 FB_B0_A<5>
FBB_CMD5 C14 FB_B0_WE_L
FBB_CMD6 B14 FB_B0_A<7>
FBB_CMD7 G15 FB_B0_A<6>
FBB_CMD8 F15 FB_B0_ABI_L
FBB_CMD9 E15 FB_B0_A<8>
FBB_CMD10 D15 FB_B0_A<0>
FBB_CMD11 A14 FB_B0_A<1>
FBB_CMD12 D14 FB_B0_RAS_L
FBB_CMD13 A15 FB_B0_RESET_L
FBB_CMD14 B15 FB_B0_CKE_L
FBB_CMD15 C17 FB_B0_CAS_L
FBB_CMD16 D18 FB_B1_CS_L
FBB_CMD17 E18 FB_B1_A<3>
FBB_CMD18 F18 FB_B1_A<2>
FBB_CMD19 A20 FB_B1_A<4>
FBB_CMD20 B20 FB_B1_A<5>
FBB_CMD21 C18 FB_B1_WE_L
FBB_CMD22 B18 FB_B1_A<7>
FBB_CMD23 G18 FB_B1_A<6>
FBB_CMD24 G17 FB_B1_ABI_L
FBB_CMD25 F17 FB_B1_A<8>
FBB_CMD26 D16 FB_B1_A<0>
FBB_CMD27 A18 FB_B1_A<1>
FBB_CMD28 D17 FB_B1_RAS_L
FBB_CMD29 A17 FB_B1_RESET_L
FBB_CMD30 B17 FB_B1_CKE_L
FBB_CMD31 E17 FB_B1_CAS_L
FBB_CLK0 D12 FB_B0_CLK_P
FBB_CLK0* E12 FB_B0_CLK_N
FBB_CLK1 E20 FB_B1_CLK_P
FBB_CLK1* F20 FB_B1_CLK_N
FBB_DQM0 E11 FB_B0_DBI_L<0>
FBB_DQM1 E3 FB_B0_DBI_L<1>
FBB_DQM2 A3 FB_B0_DBI_L<2>
FBB_DQM3 C9 FB_B0_DBI_L<3>
FBB_DQM4 F23 FB_B1_DBI_L<0>
FBB_DQM5 F27 FB_B1_DBI_L<1>
FBB_DQM6 C30 FB_B1_DBI_L<2>
FBB_DQM7 A24 FB_B1_DBI_L<3>
FBB_DQS_RN0 D9 NC
FBB_DQS_RN1 E4 NC
FBB_DQS_RN2 B2 NC
FBB_DQS_RN3 A9 NC
FBB_DQS_RN4 D22 NC
FBB_DQS_RN5 D28 NC
FBB_DQS_RN6 A30 NC
FBB_DQS_RN7 B23 NC
FBB_DQS_WP0 D10 FB_B0_EDC<0>
FBB_DQS_WP1 D5 FB_B0_EDC<1>
FBB_DQS_WP2 C3 FB_B0_EDC<2>
FBB_DQS_WP3 B9 FB_B0_EDC<3>
FBB_DQS_WP4 E23 FB_B1_EDC<0>
FBB_DQS_WP5 E28 FB_B1_EDC<1>
FBB_DQS_WP6 B30 FB_B1_EDC<2>
FBB_DQS_WP7 A23 FB_B1_EDC<3>
FBB_PLL_AVDD H17 PP1V05_GPU_FB_PLL_AVDD
FBB_DEBUG0 G14 GPU_FBB_DEBUG0
FBB_DEBUG1 G20 GPU_FBB_DEBUG1
FB_VREF H26 FB_VREF
FBB_CMD_RFU0 C12 NC
FBB_CMD_RFU1 C20 NC
C8206 1UF 20% 4V CERM-X6S 0201
C8207 0.1UF 10% 6.3V X6S 0201
=PP1V35_GPU_S0_FB
R8206 60.4 1% 1/20W MF 201
R8207 60.4 1% 1/20W MF 201
GPU_FBB_DEBUG0
GPU_FBB_DEBUG1
Page Notes
Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
L8201 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.05OHM
=PP1V05_GPU_PEX_IOVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PP1V05_GPU_FB_PLL_AVDD
C8201 20UF 20% 2V X6T-CERM 0402
C8202 1UF 20% 4V CERM-X6S 0201
C8203 0.1UF 10% 6.3V X6S 0201
FB PLL & DLL VDD
L8202 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.05OHM
=PP1V05_GPU_PEX_IOVDD
PP1V05_GPU_FB_DLL_AVDD
C8208 20UF 20% 2V X6T-CERM 0402
C8204 1UF 20% 4V CERM-X6S 0201
C8205 0.1UF 10% 6.3V X6S 0201
FB_B0_RESET_L R8254 10K 1% 1/20W MF 201
FB_B1_RESET_L R8255 10K 1% 1/20W MF 201
FB_B0_CKE_L R8256 10K 1% 1/20W MF 201
FB_B1_CKE_L R8257 10K 1% 1/20W MF 201
MEM VREFC & VREFD SWITCH
FB_SW_LEG
Q8265 SSM3K15FV SOD-VESM-HF
GPU_ALT_VREF
SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012
PAGE TITLE
KEPLER FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH
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SHEET 73 OF 99
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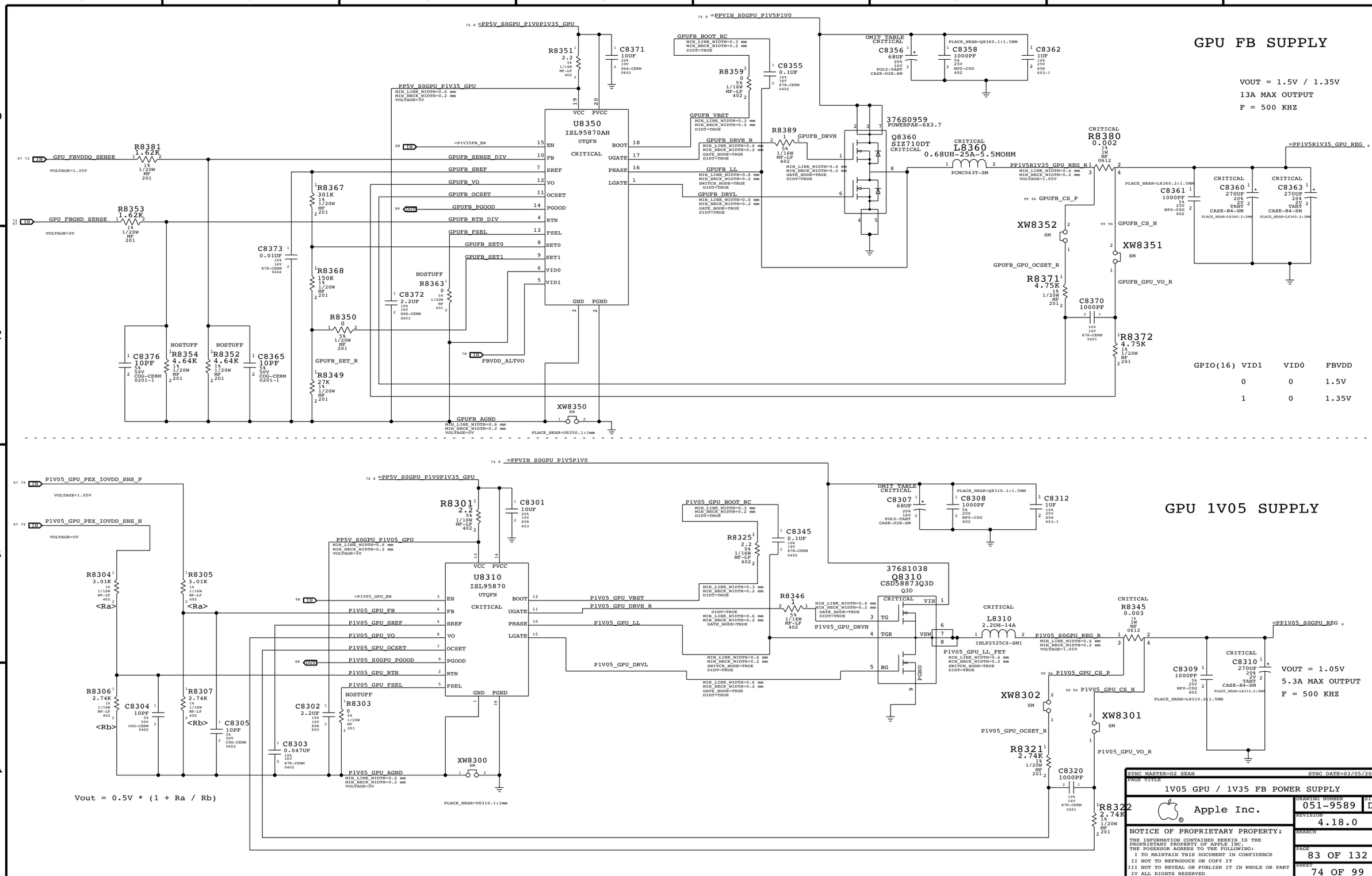
GPU FB SUPPLY
VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ
U8350
ISL95870AH
UTQFN
CRITICAL
EN
FB
SREF
VO
OCSET
PGOOD
RTN
FSEL
SET0
SET1
VID0
VID1
BOOT
UGATE
PHASE
LGATE
VCC
PVCC
GND
PGND
Q8360
SIZ710DT
CRITICAL
376S0959
POWERPAK-6X3.7
L8360
0.68UH-25A-5.5MOHM
PCMC063T-SM
GPU 1V05 SUPPLY
VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ
U8310
ISL95870
UTQFN
CRITICAL
Q8310
CSD58873Q3D
Q3D
376S1038
L8310
2.2UH-14A
IHLP2525CZ-SM1
Vout = 0.5V * (1 + Ra / Rb)
GPIO(16) VID1 VID0 FBVDD
0 0 1.5V
1 0 1.35V
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
PAGE TITLE
1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.
DRAWING NUMBER
051-9589
SIZE
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REVISION
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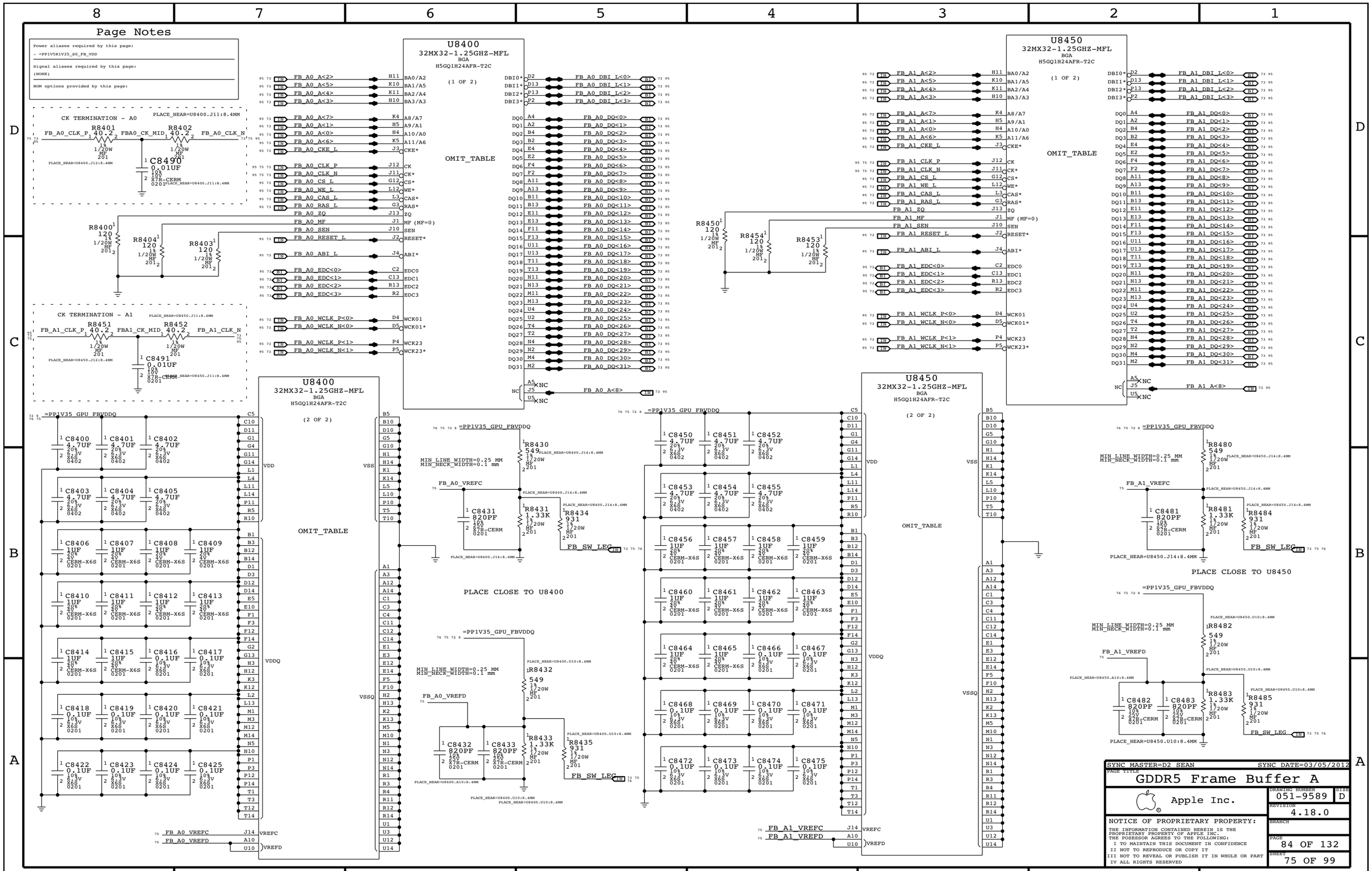
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_SO_FB_VDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE
U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE
U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE
U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE
CK TERMINATION - A0
CK TERMINATION - A1
PLACE CLOSE TO U8400
PLACE CLOSE TO U8450
=PP1V35_GPU_FBVDDQ
FB_SW_LEG
FB_A0_VREFC
FB_A0_VREFD
FB_A1_VREFC
FB_A1_VREFD
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
PAGE TITLE
GDDR5 Frame Buffer A
Apple Inc.
DRAWING NUMBER
051-9589
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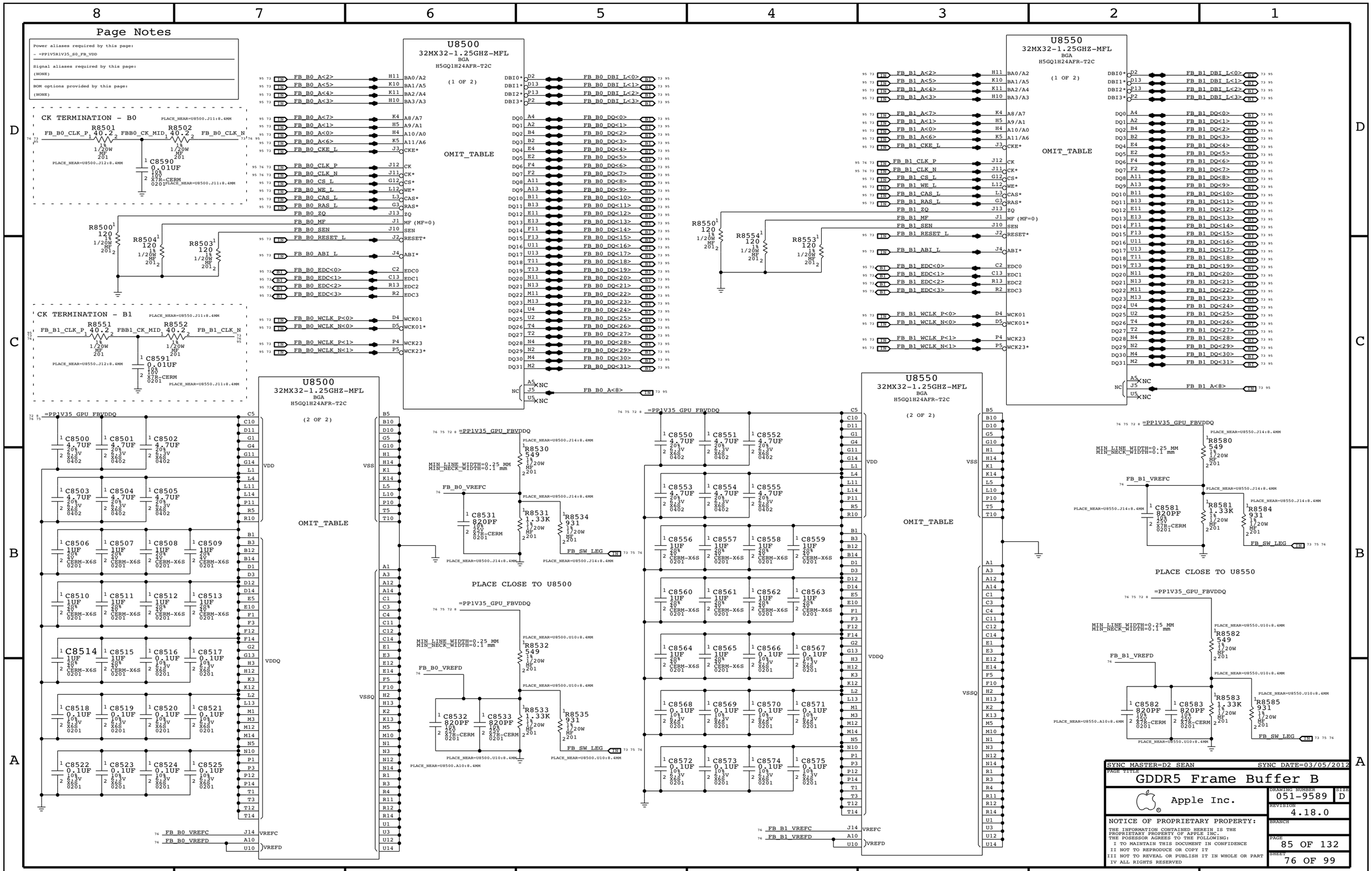
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_SO_FB_VDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
CK TERMINATION - B0
CK TERMINATION - B1
U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
OMIT_TABLE
U8550
PLACE CLOSE TO U8500
PLACE CLOSE TO U8550
=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm
GDDR5 Frame Buffer B
Apple Inc.
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
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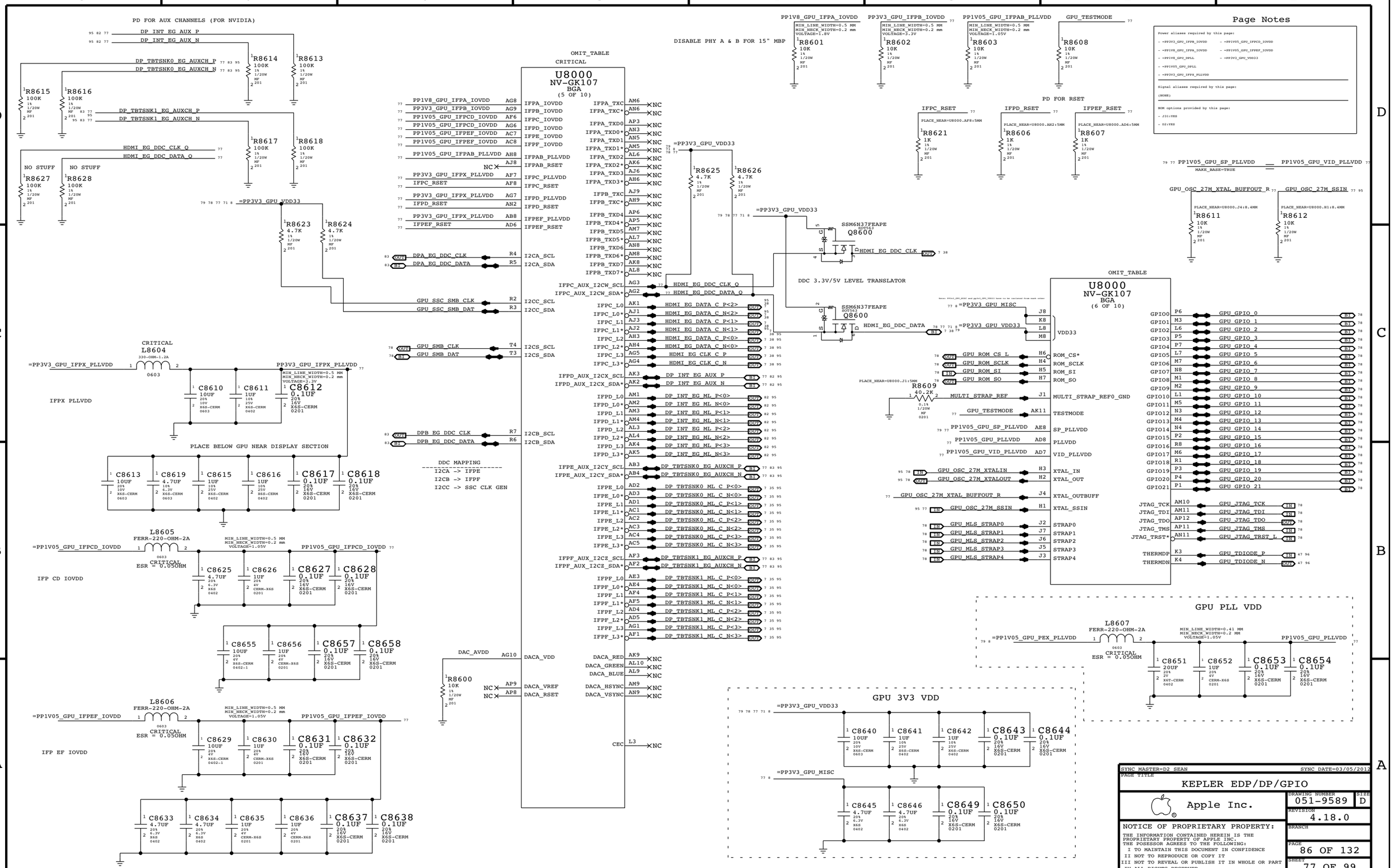

SYNC MASTER=D2_SEAN SYNC DATE=03/05/2012

PAGE TITLE

KEPLER EDP/DP/GPIO

Apple Inc.

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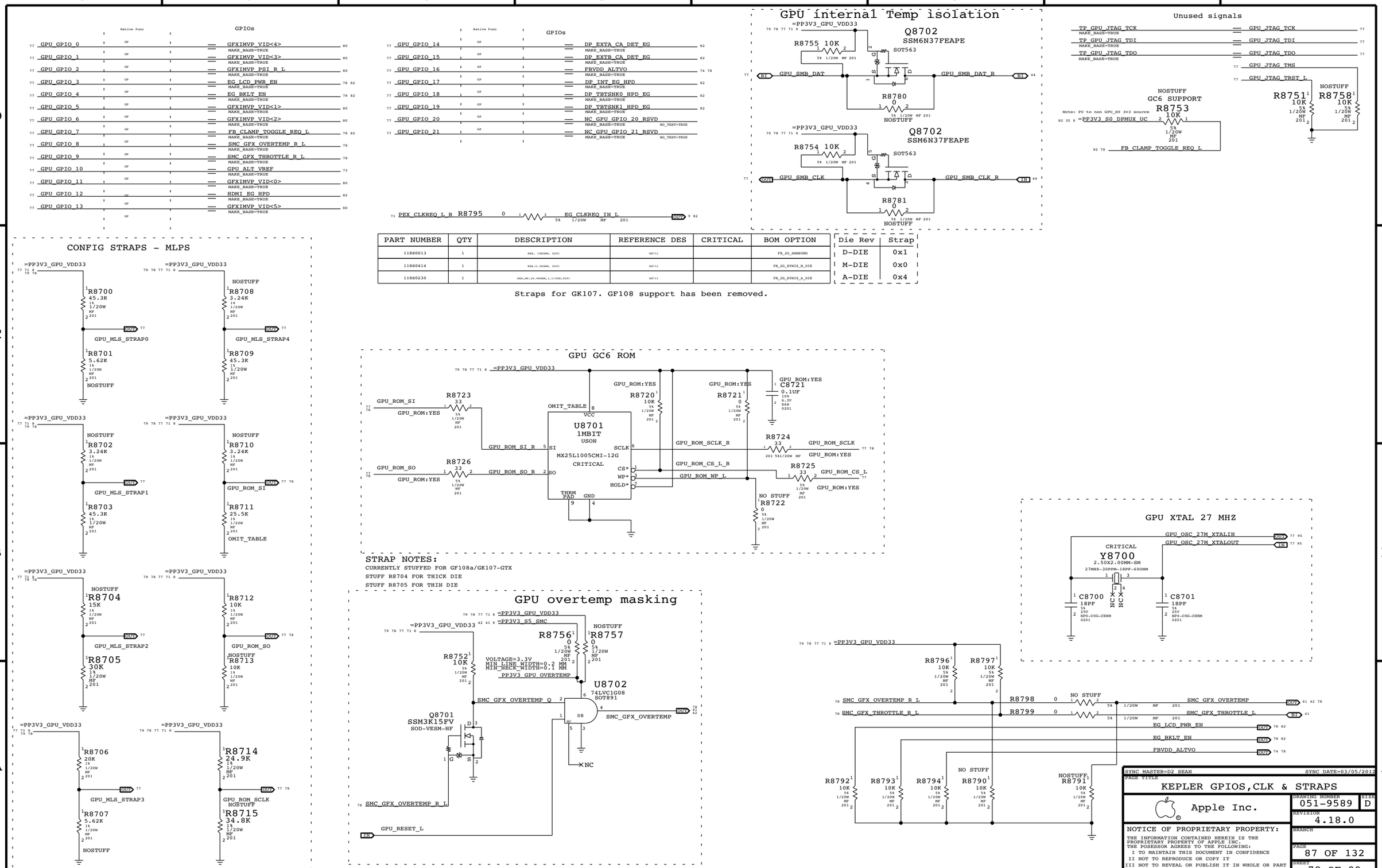
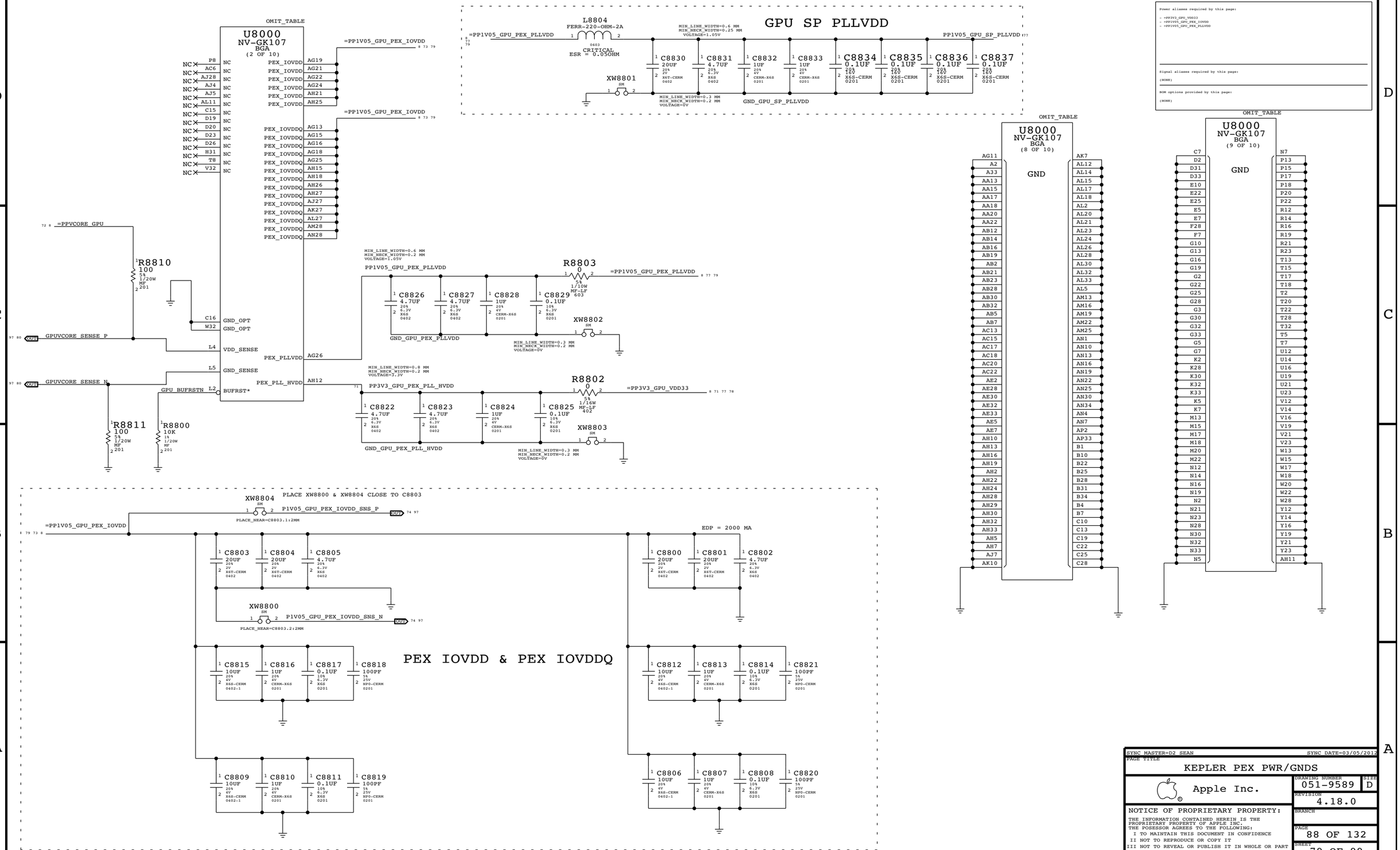


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0013	1	RES,108OHM,0201	R8711		FB_2G_SAMSUNG
118S0414	1	RES,5.18OHM,0201	R8711		FB_2G_HYNIX_M_DIE
118S0230	1	RES,MF,24.9ROHM,1,1/20W,0201	R8711		FB_2G_HYNIX_A_DIE

Die Rev	Strap
D-DIE	0x1
M-DIE	0x0
A-DIE	0x4

Straps for GK107. GF108 support has been removed.



SYNC MASTER=D2 SEAN SYNC DATE=03/05/2012

PAGE TITLE

KEPLER PEX PWR/GNDS

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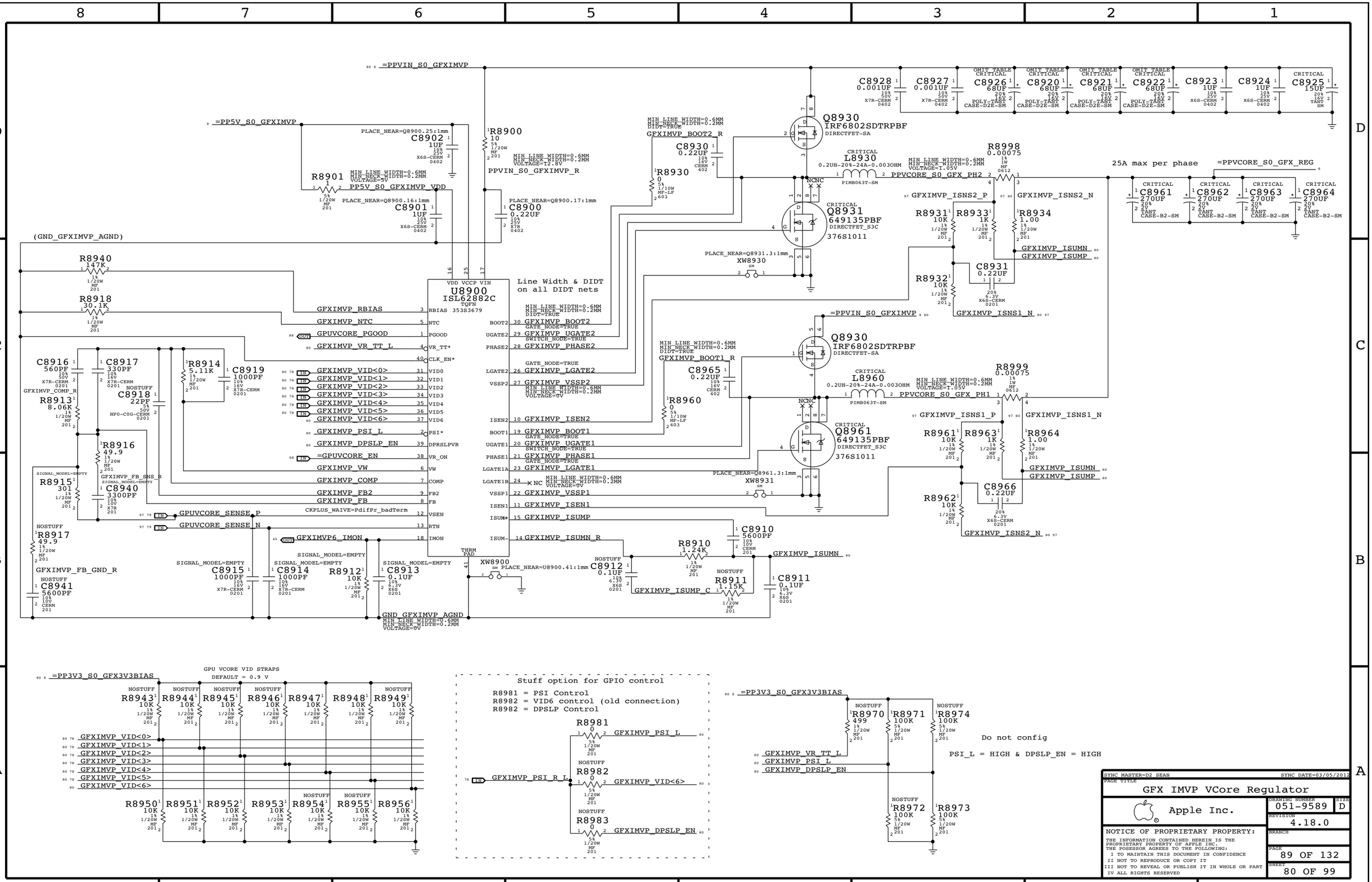
=PPVIN_S0_GFXIMVP
=PP5V_S0_GFXIMVP
(GND_GFXIMVP_AGND)
U8900
ISL62882C
TQFN
Line Width & DIDT on all DIDT nets
Q8930
IRF6802SDTRPBF
DIRECTFET-SA
Q8931
649135PBF
DIRECTFET_S3C
376S1011
Q8961
649135PBF
DIRECTFET_S3C
376S1011
L8930
L8960
PPVCORE_S0_GFX_PH2
PPVCORE_S0_GFX_PH1
25A max per phase
=PPVCORE_S0_GFX_REG
GFXIMVP_ISNS2_P
GFXIMVP_ISNS2_N
GFXIMVP_ISNS1_P
GFXIMVP_ISNS1_N
GFXIMVP_ISNS1_N
GFXIMVP_ISNS2_N
GFXIMVP_ISUMN
GFXIMVP_ISUMP
GFXIMVP_ISUMN_R
GFXIMVP_ISUMN
GFXIMVP_ISUMP_C
GFXIMVP_RBIAS
GFXIMVP_NTC
GPUVCORE_PGOOD
GFXIMVP_VR_TT_L
GFXIMVP_VID<0>
GFXIMVP_VID<1>
GFXIMVP_VID<2>
GFXIMVP_VID<3>
GFXIMVP_VID<4>
GFXIMVP_VID<5>
GFXIMVP_VID<6>
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN
=GPUVCORE_EN
GFXIMVP_VW
GFXIMVP_COMP
GFXIMVP_FB2
GFXIMVP_FB
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GFXIMVP6_IMON
GFXIMVP_BOOT2
GFXIMVP_UGATE2
GFXIMVP_PHASE2
GFXIMVP_LGATE2
GFXIMVP_VSSP2
GFXIMVP_ISEN2
GFXIMVP_BOOT1
GFXIMVP_UGATE1
GFXIMVP_PHASE1
GFXIMVP_LGATE1
GFXIMVP_VSSP1
GFXIMVP_ISEN1
GFXIMVP_ISUMP
GFXIMVP_BOOT2_R
GFXIMVP_BOOT1_R
GND_GFXIMVP_AGND
GPU VCORE VID STRAPS
DEFAULT = 0.9 V
=PP3V3_S0_GFX3V3BIAS
Stuff option for GPIO control
R8981 = PSI Control
R8982 = VID6 control (old connection)
R8982 = DPSLP Control
GFXIMVP_PSI_R_L
Do not config
PSI_L = HIGH & DPSLP_EN = HIGH
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
PAGE TITLE
GFX IMVP VCore Regulator
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
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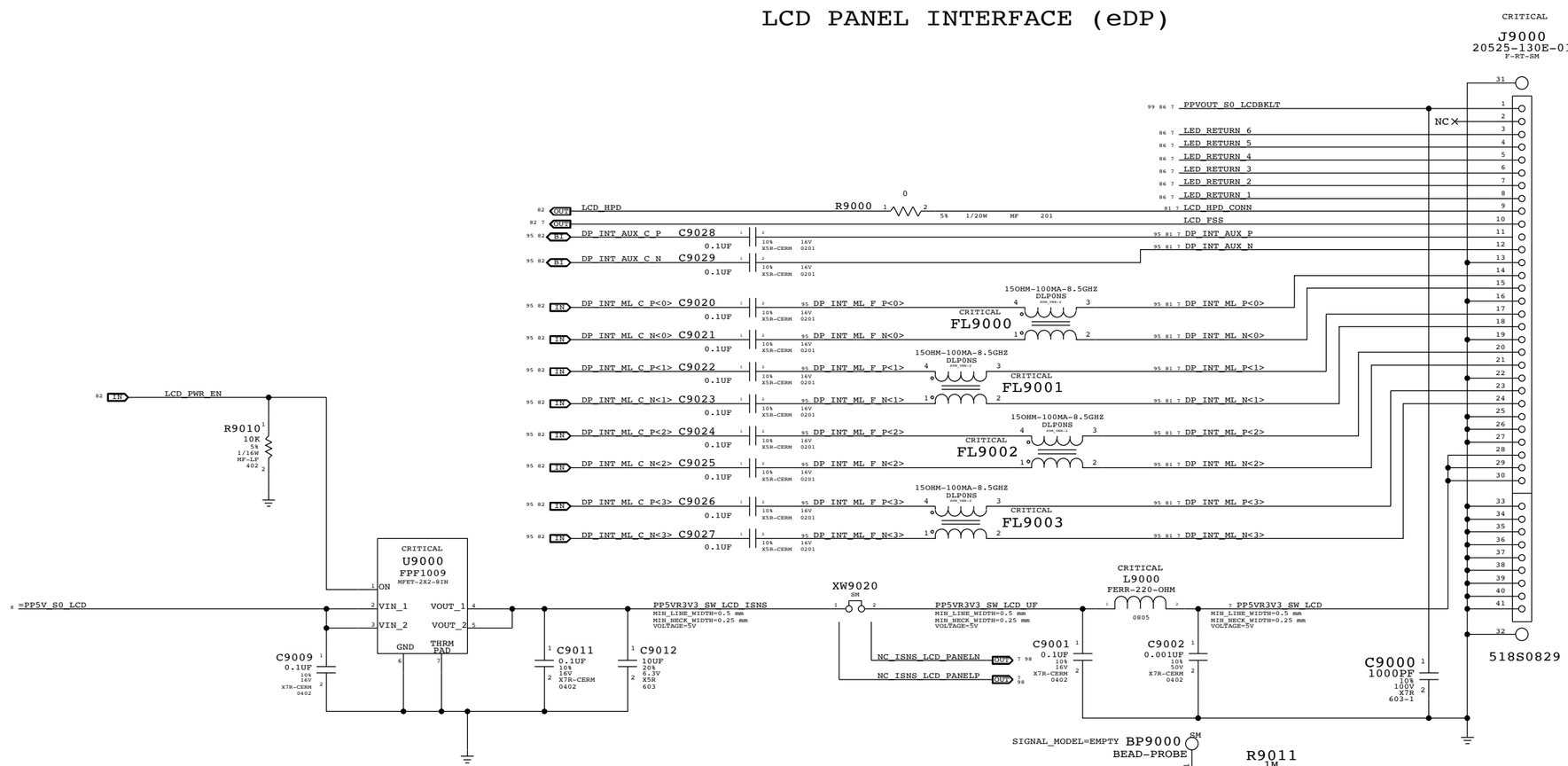
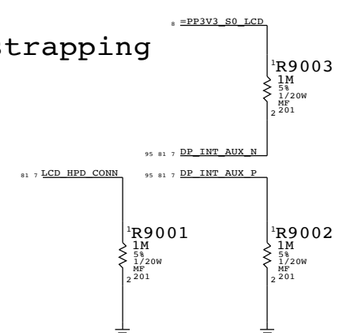
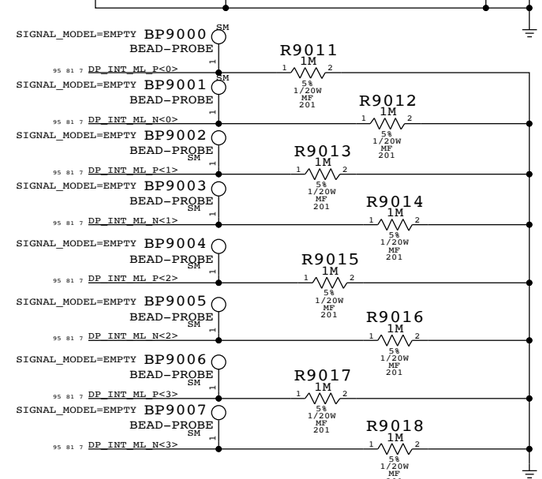
LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping





SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

eDP Display Connector

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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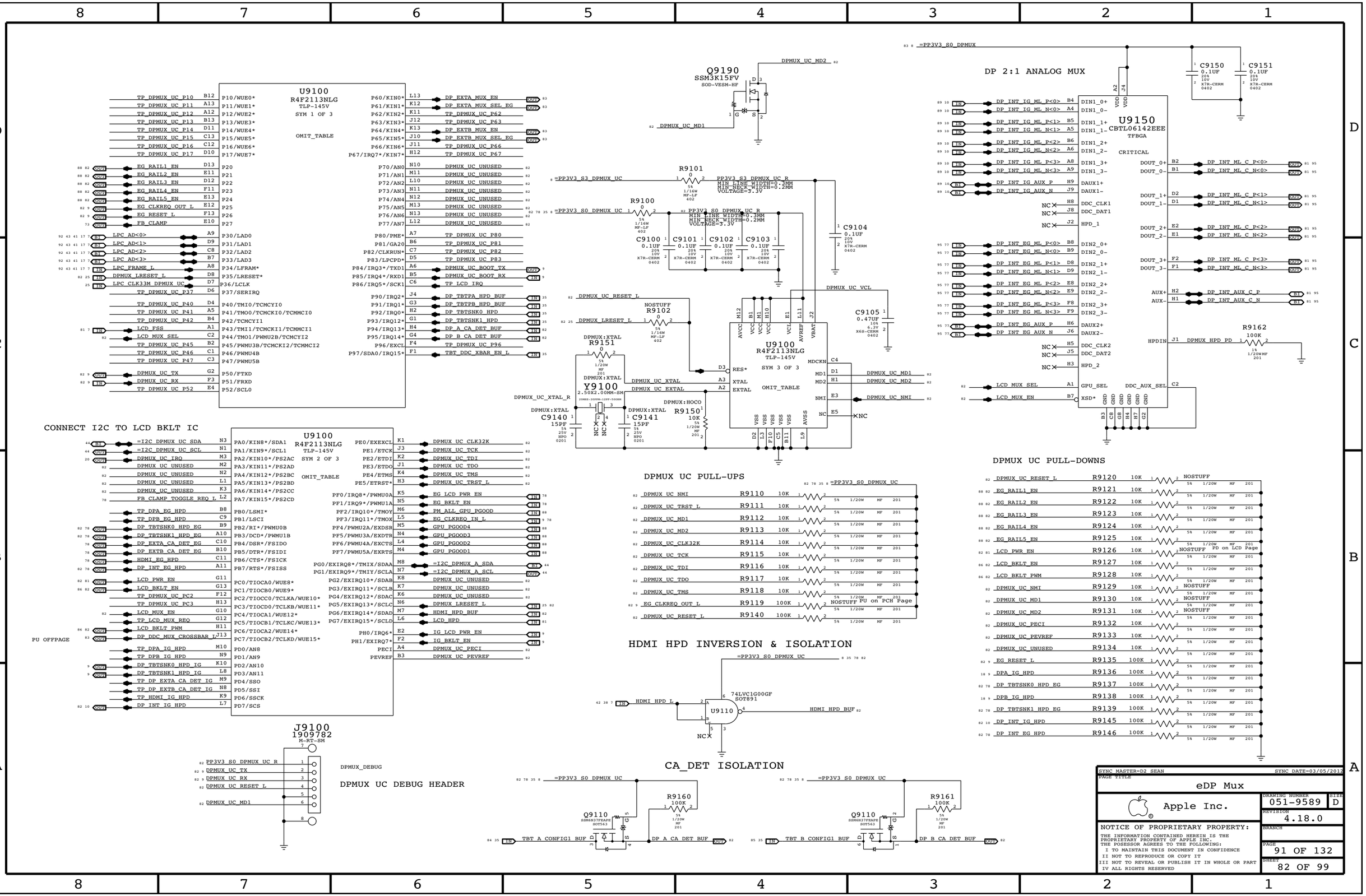
U9100
R4F2113NLG
TLP-145V
SYM 1 OF 3
OMIT_TABLE
U9100
R4F2113NLG
TLP-145V
SYM 2 OF 3
OMIT_TABLE
CONNECT I2C TO LCD BKLT IC
PU OFFPAGE
Q9190
SSM3K15FV
SOD-VESM-HF
DPMUX UC PULL-UPS
U9100
R4F2113NLG
TLP-145V
SYM 3 OF 3
OMIT_TABLE
DP 2:1 ANALOG MUX
U9150
CBTL06142EEE
TFBGA
CRITICAL
DPMUX UC PULL-DOWNS
HDMI HPD INVERSION & ISOLATION
74LVC1G00GF
SOT891
CA_DET ISOLATION
J9100
1909782
M-RT-SM
DPMUX_DEBUG
DPMUX UC DEBUG HEADER
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
PAGE TITLE
eDP Mux
Apple Inc.
DRAWING NUMBER
051-9589
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D
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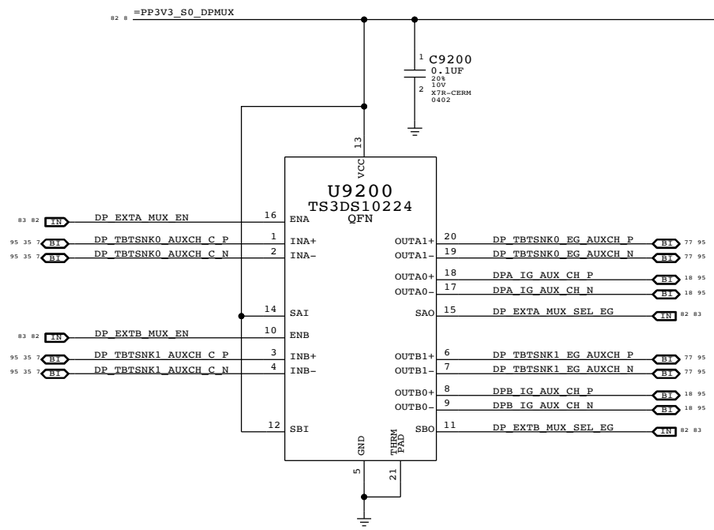
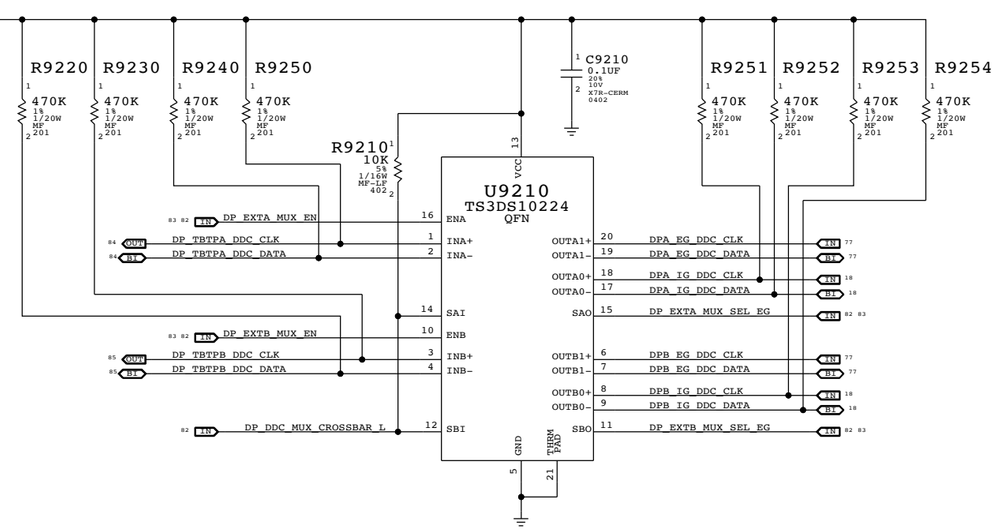
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC MASTER=D2 SEAN SYNC DATE=03/05/2012

PAGE TITLE
eDP Muxed Graphics Support

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DRAWING NUMBER 051-9589 SIZE D

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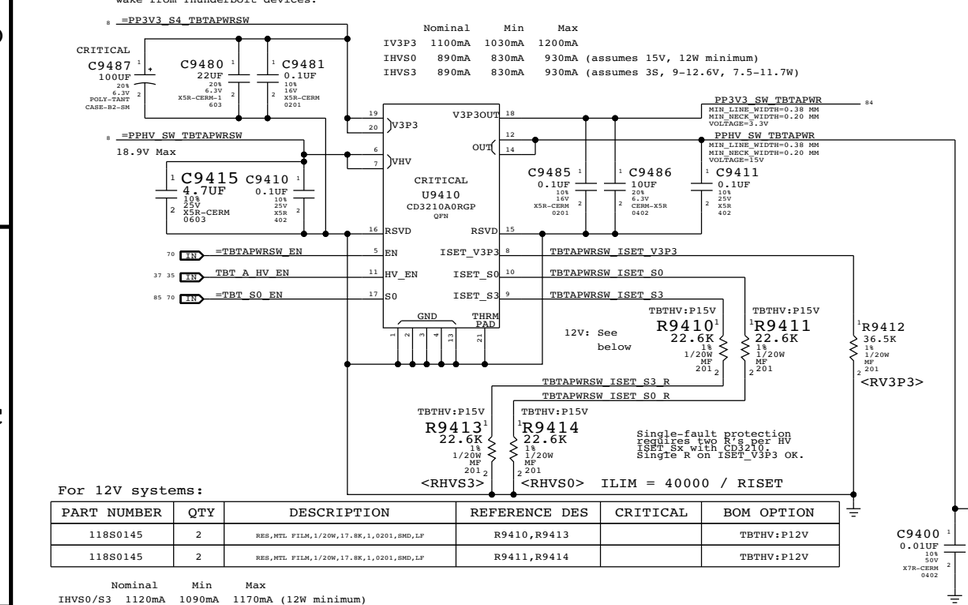
3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

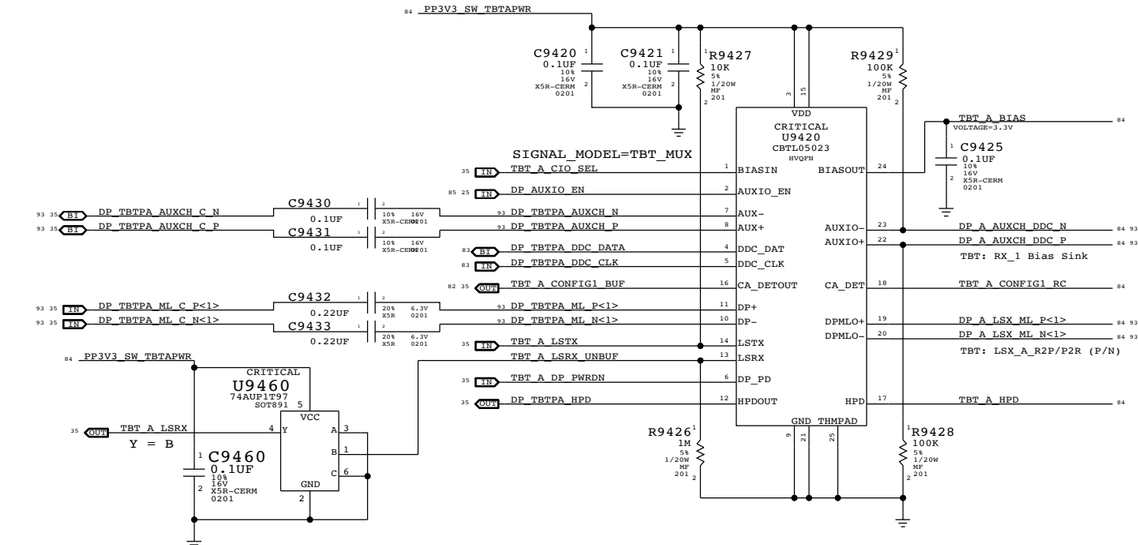
	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)



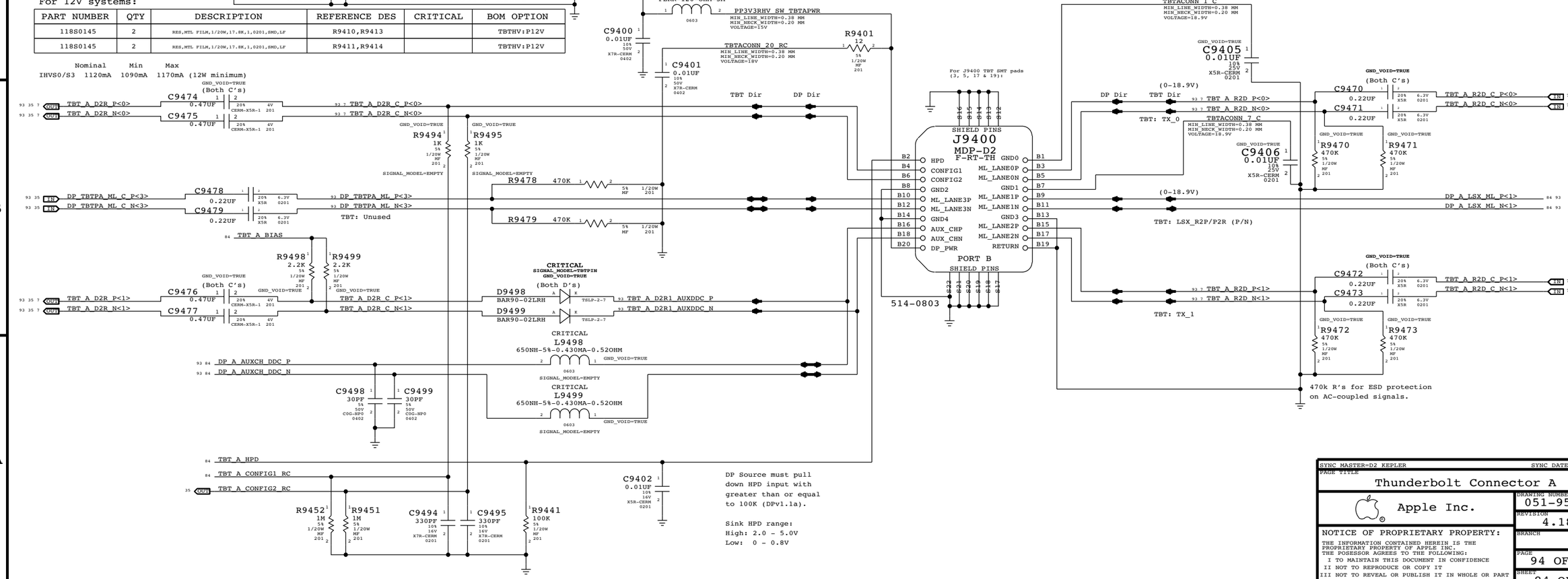
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)



Thunderbolt Connector A



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE: Thunderbolt Connector A

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DRAWING NUMBER: 051-9589 SIZE: D

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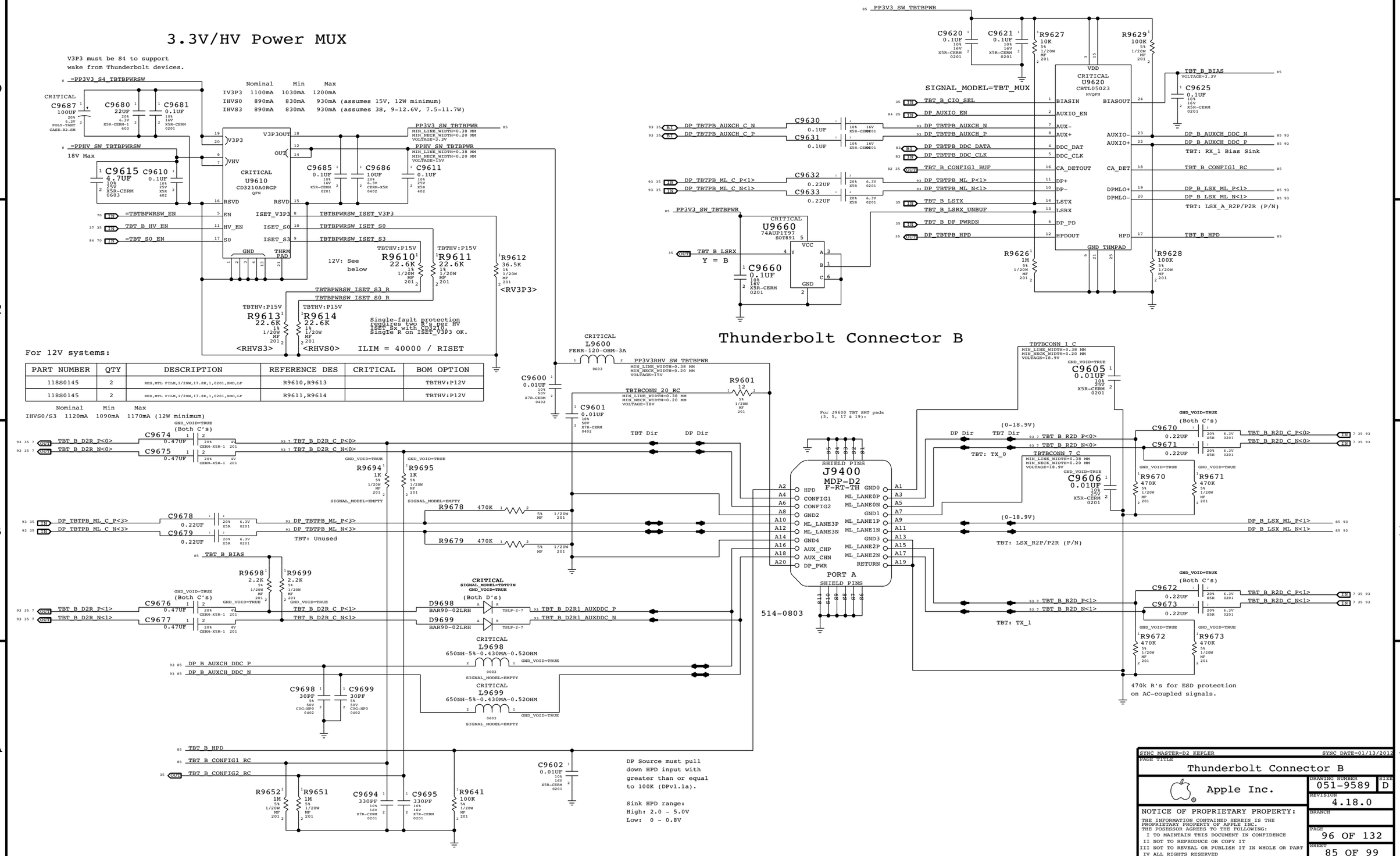
3.3V/HV Power MUX
V3P3 must be S4 to support wake from Thunderbolt devices.
Nominal Min Max
IV3P3 1100mA 1030mA 1200mA
IHVS0 890mA 830mA 930mA (assumes 15V, 12W minimum)
IHVS3 890mA 830mA 930mA (assumes 3S, 9-12.6V, 7.5-11.7V)
=PP3V3_S4_TBTBPWRSW
=PPHV_SW_TBTBPWRSW
18V Max
CRITICAL
C9687 100UF
C9680 22UF
C9681 0.1UF
C9615 4.7UF
C9610 0.1UF
CRITICAL
U9610
CD3210A0RGP
QFN
V3P3
VHV
V3P3OUT
OUT
RSVD
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
PP3V3_SW_TBTBPWR
PPHV_SW_TBTBPWR
C9685 0.1UF
C9686 10UF
C9611 0.1UF
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V
R9610 22.6K
R9611 22.6K
12V: See below
R9612 36.5K
<RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R9613 22.6K
R9614 22.6K
<RHVS3>
<RHVS0>
Single-fault protection requires two R's per HV ISET Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET
For 12V systems:
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
118S0145 | 2 | RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF | R9610,R9613 | | TBTHV:P12V
118S0145 | 2 | RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF | R9611,R9614 | | TBTHV:P12V
Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)
Thunderbolt Connector B
SIGNAL_MODEL=TBT_MUX
PP3V3_SW_TBTBPWR
C9620 0.1UF
C9621 0.1UF
R9627 10K
R9629 100K
VDD
CRITICAL
U9620
CBTL05023
HVQFN
TBT_B_BIAS
C9625 0.1UF
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C9630 0.1UF
C9631 0.1UF
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
C9632 0.22UF
C9633 0.22UF
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN
DP_TBTPB_HPD
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND THMPAD
DP_B_AUXCH_DDC_N
DP_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD
R9626 1M
R9628 100K
CRITICAL
U9660
74AUP1T97
SOT891
VCC
GND
TBT_B_LSRX
Y = B
C9660 0.1UF
CRITICAL
L9600
FERR-120-OHM-3A
PP3V3RHV_SW_TBTBPWR
C9600 0.01UF
C9601 0.01UF
TBTBCONN_20_RC
R9601 12
TBT Dir
DP Dir
For J9600 TBT SMT pads (3, 5, 17 & 19):
SHIELD PINS
J9400
MDP-D2
F-RT-TH
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT A
514-0803
TBTBCONN_1_C
C9605 0.01UF
(0-18.9V)
TBT: TX_0
TBTBCONN_7_C
C9606 0.01UF
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1
C9670 0.22UF
C9671 0.22UF
R9670 470K
R9671 470K
C9672 0.22UF
C9673 0.22UF
R9672 470K
R9673 470K
(Both C's)
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
C9674 0.47UF
C9675 0.47UF
C9676 0.47UF
C9677 0.47UF
R9694 1K
R9695 1K
SIGNAL_MODEL=EMPTY
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
C9678 0.22UF
C9679 0.22UF
TBT: Unused
R9678 470K
R9679 470K
R9698 2.2K
R9699 2.2K
CRITICAL
SIGNAL_MODEL=TBTPIN
GND_VOID=TRUE
(Both D's)
D9698 BAR90-02LRH
D9699 BAR90-02LRH
TSLP-2-7
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
CRITICAL
L9698
650NH-5%-0.430MA-0.52OHM
CRITICAL
L9699
650NH-5%-0.430MA-0.52OHM
DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C9698 30PF
C9699 30PF
470k R's for ESD protection on AC-coupled signals.
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R9652 1M
R9651 1M
C9694 330PF
C9695 330PF
R9641 100K
C9602 0.01UF
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
SYNC MASTER=D2 KEPLER
SYNC DATE=01/13/2012
PAGE TITLE
Thunderbolt Connector B
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
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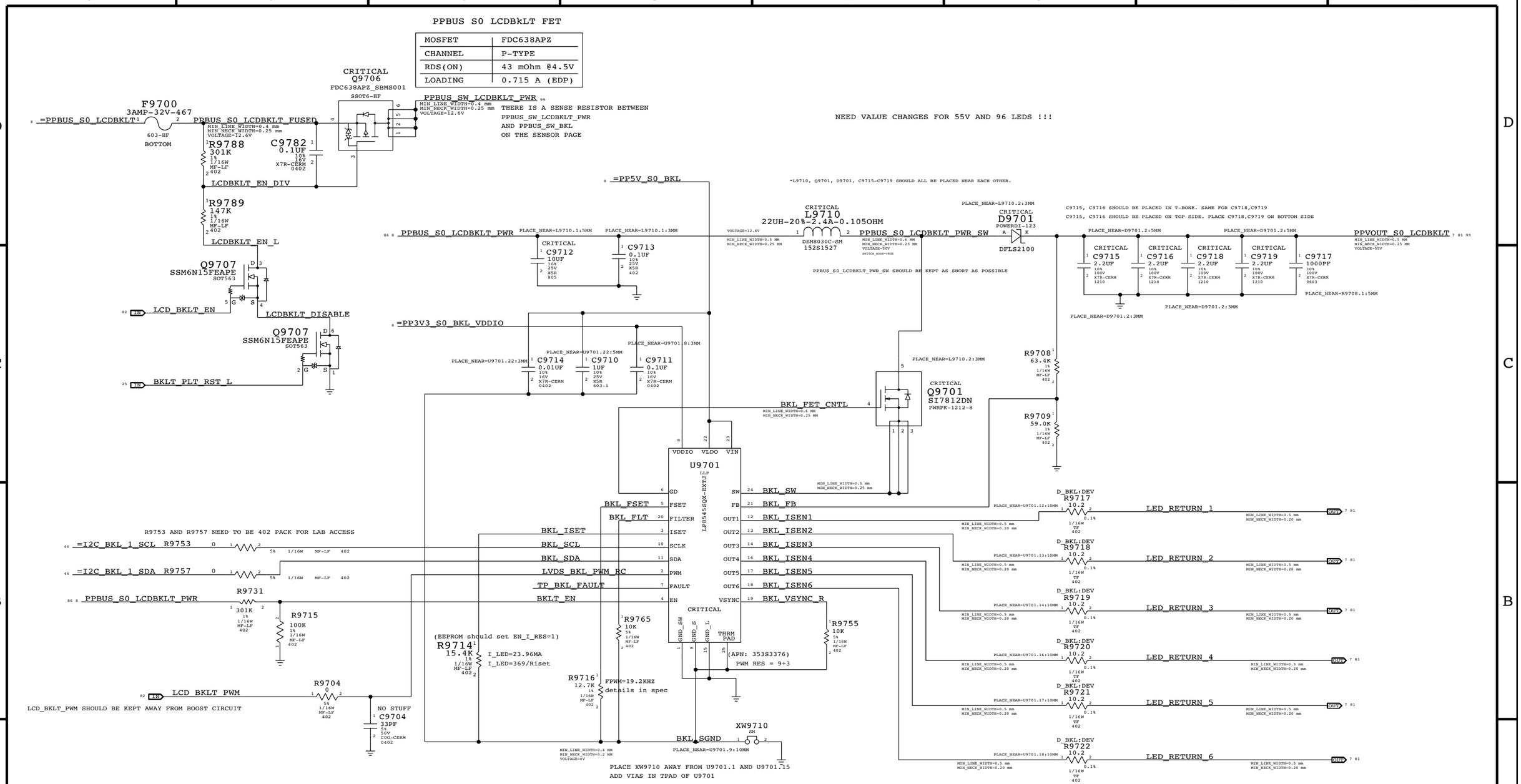

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES, 0OHM, 0402	R9717,R9718,R9719,R9720,R9721,R9722		D_BKL:PROD

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
LCD Backlight Driver (LP8545)

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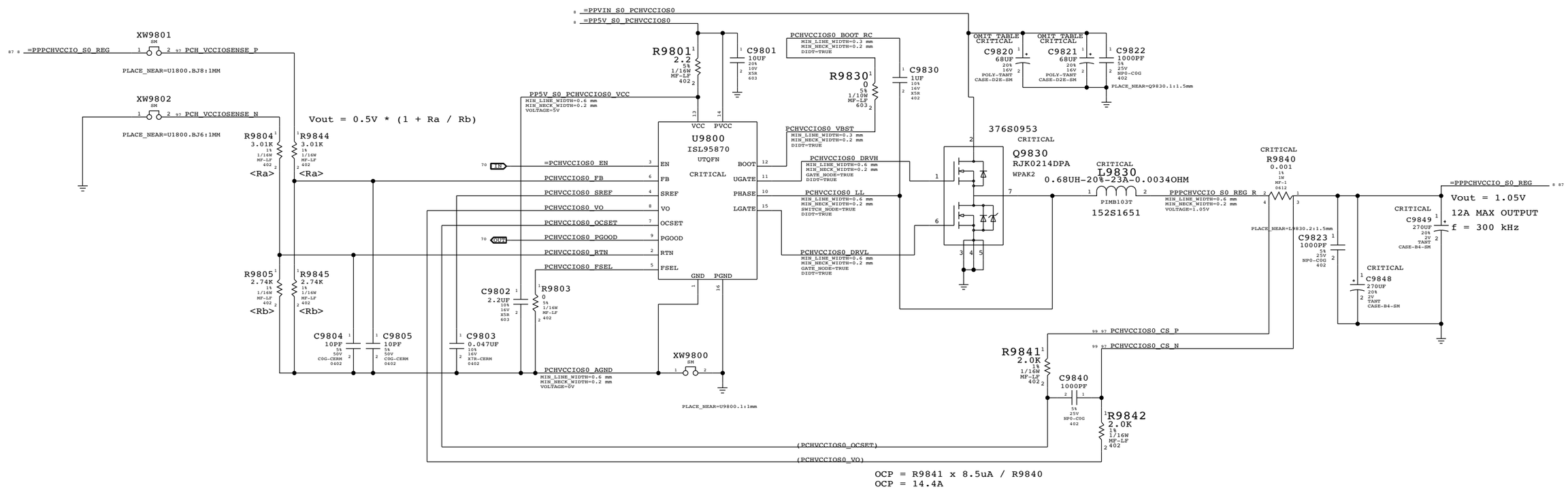
PCH VCCIO (1.05V S0) REGULATOR



OCP = R9841 x 8.5uA / R9840
OCP = 14.4A

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

PCH VCCIO (1.05V) POWER SUPPLY

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GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

1) GPU_3.3V
2) IFPX IOVDD - 1.8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IFPY IOVDD - 1.05V

82	EG_RAIL1_EN	P3V3GPU_EN (MAKE_BASE=TRUE)	=P3V3GPU_MISC_EN	OUT 69
			=P3V3GPU_EN	OUT 69
82	EG_RAIL2_EN	P1V8GPU_EN (MAKE_BASE=TRUE)	=P1V8GPU_EN	OUT 8
82	EG_RAIL3_EN	GPUVCORE_EN (MAKE_BASE=TRUE)	=GPUVCORE_EN	OUT 80
82	EG_RAIL4_EN	P1V35GPUFB_EN (MAKE_BASE=TRUE)	=P1V35FB_EN	OUT 74
82	EG_RAIL5_EN	P1V05_S0GPU_EN (MAKE_BASE=TRUE)	=P1V05_GPU_EN	OUT 74

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

88 70 8 =PP3V3_S0_PWRCTL

R9900 100K 5% 1/20W MF 201
R9901 100K 5% 1/20W MF 201
R9902 100K 5% 1/20W MF 201

69 8	IN =PP3V3_S0GPU_FET	GPU_PGOOD1	OUT 82
8	IN =PP1V8_GPU_FET	GPU_PGOOD2	OUT 82
80	IN GPUVCORE_PGOOD (MAKE_BASE=TRUE)	GPU_PGOOD3	OUT 82
74	IN GPUFB_PGOOD (MAKE_BASE=TRUE)	GPU_PGOOD4	OUT 82
74	IN P1V05_S0GPU_PGOOD (MAKE_BASE=TRUE)	PM_ALL_GPU_PGOOD	OUT 82

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

Unused PGOOD signal

88 70 8 =PP3V3_S0_PWRCTL

NO STUFF
R9991 10K 5% 1/16W MF-LF 402

	CPUIMVP_AKG_PGOOD	IN 65
TP_DDRREG_PGOOD (MAKE_BASE=TRUE)	DDRREG_PGOOD	IN 84
TP_P1V563R60_RAMP_DONE (MAKE_BASE=TRUE)	P1V563R60_RAMP_DONE	IN 69

PEG_R2D_P<0> 71 89 — R9910 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<0> 71 89

PEG_R2D_P<5> 71 89 — R9915 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<5> 71 89

PEG_R2D_P<3> 71 89 — R9913 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<3> 71 89

PEG_R2D_P<7> 71 89 — R9917 82 5% 1/20W MF 201 — NOSTUFF — PEG_R2D_N<7> 71 89

PLACE R9910 - R9917 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> 9 71 89 — R9920 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<0> 9 71 89

PEG_D2R_P<4> 9 71 89 — R9924 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<4> 9 71 89

PEG_D2R_P<7> 9 71 89 — R9927 82 5% 1/20W MF 201 — NOSTUFF — PEG_D2R_N<7> 9 71 89

PLACE R9920 - R9927 CLOSE TO U1000

SYNC MASTER=D2 KEPLER — SYNC DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=4X_DIELECTRIC	?
PEG_TXTX	*	=4X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 10
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 10
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 10
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 10
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	10 82
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	10 82
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	10 82
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	10 82
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	9 11
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	9 11
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 41
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 42
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 41 42 65
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 42
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 65
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 65
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 65
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	13
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 62
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 33
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 29 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	30 31 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 29 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	30 31 33
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	71 88
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	71 88
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	9 71
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	9 71
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	71
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	71

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

DDR3 (Memory Down):
DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	12 28 29 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..2>	
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..2>	
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 29 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 28 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 28 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 28 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 28 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 28 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	12 30 31 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..2>	
MEM_B_CNTL1	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 30 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..1>	12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_ODT<0>	12 30 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..7>	12 30 31 32
MEM_B_CMD6	MEM_40S	MEM_CMD	MEM_B_A<6>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<5..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 30 31 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 30 31
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 30 31
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 30 31
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 30 31
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 30 31
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 30 31
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 30 31
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 30 31

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	1HS,1H6,1H9,1H10	=4:1_SPACING	?
LVDS	1HS,1H6,1H9,1H10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	1HS,1H6,1H9,1H10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	1HS,1H6,1H9,1H10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	1HS,1H6,1H9,1H10	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	9 18
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	9 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 39
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 39
	SATA_90D	SATA	SATA_HDD_D2R_N	17 39
SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_P	39
	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_N	39
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_P	39
	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_N	39
1233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSD_D2R_P	39
1233	SATA_90D	SATA	SATA_SSD_D2R_N	39
1233 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_P	39
1233	SATA_90D	SATA	SATA_SSD_R2D_N	39
1218 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	
1218	SATA_90D	SATA	SATA_HDD_R2D_UF_N	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 17
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 17
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 17
	SATA_90D	SATA	SATA_ODD_D2R_N	9 17
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
1213 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	17
1233 USB_HUB1_UP	USB_85D	USB	USB_EXTB_XHCI_P	19 26
1233	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_HUB1_UP	USB_85D	USB	USB_EXTB_EHCI_P	19 26
	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 40
	USB_85D	USB	USB_EXTA_N	19 40
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 38
	USB_85D	USB	USB_EXTB_N	7 26 38
USB_EXTC	USB_85D	USB	USB_EXTC_P	9 19
	USB_85D	USB	USB_EXTC_N	9 19
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 34
	USB_85D	USB	USB_CAMERA_CONN_N	7 34
USB_BT	USB_85D	USB	USB_BT_P	9 34
	USB_85D	USB	USB_BT_N	9 34
USB_BT	USB_85D	USB	USB_BT_CONN_P	7 34
	USB_85D	USB	USB_BT_CONN_N	7 34
1260 USB_BT	USB_85D	USB	USB_BT_WAKE_P	34
1259	USB_85D	USB	USB_BT_WAKE_N	34
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 49
	USB_85D	USB	USB_TPAD_N	9 49
USB_TR	USB_85D	USB	USB_SMC_P	9 41
	USB_85D	USB	USB_SMC_N	9 41
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
1233 USB_T29A	USB_85D	USB	USB_EXTD_XHCI_P	19 26
1233	USB_85D	USB	USB_EXTD_XHCI_N	19 26
1243 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	40
1243	USB_85D	USB	USB_EXTA_MUXED_N	40
1243 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 34
1243	USB_85D	USB	USB_CAMERA_N	19 34
1243 USB_EXTA	USB_85D	USB	USB_LT1_P	40
1243	USB_85D	USB	USB_LT1_N	40
1222 USB3_EXTB_TX	USB_85D	USB3	USB3_EXTB_TX_P	19 38
1222	USB_85D	USB3	USB3_EXTB_TX_N	19 38
1222 USB3_EXTB_RX	USB_85D	USB3	USB3_EXTB_RX_P	7 19 38
1222	USB_85D	USB3	USB3_EXTB_RX_N	7 19 38
1222 USB3_EXTC_TX	USB_85D	USB3	USB3_EXTC_TX_P	9 19
1222	USB_85D	USB3	USB3_EXTC_TX_N	9 19
1222 USB3_EXTC_RX	USB_85D	USB3	USB3_EXTC_RX_P	9 19
1222	USB_85D	USB3	USB3_EXTC_RX_N	9 19
1233 USB3_EXTA_TX	USB_85D	USB3	USB3_EXTA_TX_P	19 40
1222	USB_85D	USB3	USB3_EXTA_TX_N	19 40
1222 USB3_EXTA_RX	USB_85D	USB3	USB3_EXTA_RX_P	19 40
1233	USB_85D	USB3	USB3_EXTA_RX_N	19 40

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1255 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
1255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
1255	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
1255 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
1255	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
1255 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 35
1255	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	35

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PCH Constraints 1

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 41 43 82
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 41 43 82
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 53
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 53
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 53
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 53
	HDA_50S	HDA	AUD_SDI_R	53
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 53
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 43
	SPI_55S	SPI	SPI_CLK	43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 43
	SPI_55S	SPI	SPI_MOSI	43
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 43
	SPI_55S	SPI	SPI_CS0_L	43
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 38
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 34
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 34
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	17 34
	PCIE_85D	PCIE	PCIE_AP_D2R_N	17 34
(127) PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 34
(127)	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 34
(127) PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	34
(127)	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	34
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_P	39
	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_N	39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_C_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_R2D_C_N<1..0>	9 39
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_P<1..0>	9 39
	PCIE_85D	PCIE	PCIE_SSD_D2R_N<1..0>	9 39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_P	39
	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_N	39
(127) PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_C_P<1>	39
(127)	PCIE_85D	PCIE	PCIE_SSD_D2R_C_N<1>	39
(127) PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_P<1>	39
(127)	PCIE_85D	PCIE	PCIE_SSD_R2D_N<1>	39
(253) PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17
(254)	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17
(262) PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	17 35
(261)	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	17 35
(255)	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
(257)	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
(256) PCIE_CLK100M_TBT_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17
(259)	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
(258)	CMOS_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
(260)	CMOS_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 25
(127) PCIE_CLK100M	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_P	71 95
(128)	1:1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_N	71 95
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 71
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 71
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 38
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 34
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	9 17
(128) PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	17 39
(128)	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	17 39
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
(263) PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	9 35
(264) PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	9 35
(265) PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	35
(267) PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	35
(266) PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	9 35
(268) PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	9 35
(270) PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	35
(269) PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	35

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PCH Constraints 2

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TBTDP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 35 84
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 35 84
	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	35 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1..0>	7 84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1..0>	7 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_P<1..0>	7 35 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_N<1..0>	7 35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	84
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 35 85
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 35 85
	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	35 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1..0>	7 85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1..0>	7 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_P<1..0>	7 35 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_N<1..0>	7 35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	85
	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	85

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	35
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	35
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	35
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	35

Only used on hosts supporting Thunderbolt video-in

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Thunderbolt Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 41 44
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 41 44
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	61
	1TO1_DIFFPAIR		CHGR_CSI_N	61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	61
	1TO1_DIFFPAIR		CHGR_CSO_N	61

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1455	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	73 75
1456	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	73 75
1450	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	73 75
1451	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	73 75
1450	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	73 75
1445	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	73 75
1443	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	73 75
1444	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	73 75
1449	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	73 75
1448	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	73 75
1442	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	73 75
1441	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	73 75
1440	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	73 75
1439	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	73 75
1444	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	73 75
1437	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	73 75
1437	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	73 75
1438	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	73 75
1439	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	73 75
1437	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	73 75
1400	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	73 75
1400	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	73 75
1400	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	73 75
1399	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	73 75
1399	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	73 75
1399	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	73 75
1393	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	73 75
1392	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	73 75
1392	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	73 75
1392	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	73 75
1392	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	73 75
1390	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	73 75
1391	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	73 75
1389	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	73 75
1388	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	73 75
1387	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	73 75
1385	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	73 75
1386	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	73 75
1383	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	73 75
1384	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	73 75
1382	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	73 75
1380	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	73 75
1381	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	73 75
1372	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	73 75
1372	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	73 75
1377	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	73 75
1372	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	73 75
1372	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	73 75
1372	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	73 75
1377	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	73 75
1377	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	73 75
1377	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	73 75

GDDR5 FB B Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1472	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	73 76
1473	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	73 76
1472	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	73 76
1470	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	73 76
1471	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	73 76
1466	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	73 76
1466	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	73 76
1466	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	73 76
1466	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	73 76
1466	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	73 76
1466	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	73 76
1466	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	73 76
1466	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	73 76
1466	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	73 76
1466	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	73 76
1465	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	73 76
1455	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	73 76
1455	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	73 76
1455	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	73 76
1455	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	73 76
1433	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	73 76
1433	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	73 76
1433	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	73 76
1430	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	73 76
1433	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	73 76
1429	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	73 76
1428	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	73 76
1427	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	73 76
1428	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	73 76
1428	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	73 76
1428	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	73 76
1427	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	73 76
1428	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	73 76
1424	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	73 76
1422	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	73 76
1421	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	73 76
1421	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	73 76
1421	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	73 76
1419	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	73 76
1419	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	73 76
1419	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	73 76
1419	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	73 76
1418	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	73 76
1418	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	73 76
1418	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	73 76
1408	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	73 76
1408	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	73 76
1408	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	73 76
1408	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	73 76
1408	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	73 76
1408	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	73 76
1408	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	73 76

MUXGFX & DP AUX MUX NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	81 82
		DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	81 82
	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	81 82
		DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	81 82
1347	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 81
1348		DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 81
1349	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	77 82
1350		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	77 82
1341	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	7 81
1342		DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	7 81
1343	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	81
1344		DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	81
1345	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	77 82
1346		DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	77 82
1332	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	18 83
1333		DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	18 83
1330	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	18 83
1335		DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	18 83
1330	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P	77 83
1333		DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N	77 83
1331	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P	77 83
1340		DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N	77 83
1351	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	7 35 83
1352		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	7 35 83
1353	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	7 35 83
1354		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	7 35 83
1355	DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	7 35 77
1356		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	7 35 77
1363	DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	7 35 77
1364		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	7 35 77
1357	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	7 35
1358		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	7 35
1359	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	7 35
1361		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	7 35
1360	DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	7 35
1362		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	7 35
1365	DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	7 35
1366		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	7 35

Kepler Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALIN	77 78
	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALOUT	77 78
	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT	
	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_SSIN	77
		1:1_DIFFPAIR		PEX_TSTCLK_O_P	71 92
		1:1_DIFFPAIR		PEX_TSTCLK_O_N	71 92
	HDMI_DATA	HDMI_90D	HDMI	HDMI_EG_DATA_C_P<2..0>	7 38 77
		HDMI_90D	HDMI	HDMI_EG_DATA_C_N<2..0>	7 38 77
	HDMI_CLK	HDMI_90D	HDMI	HDMI_EG_CLK_C_P	7 38 77
		HDMI_90D	HDMI	HDMI_EG_CLK_C_N	7 38 77

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_55S_CPUIMVPISNS1	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	47
	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 77
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 77
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	45 62
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	45 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	45
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_P	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIO80_CS_P	45 67
	SENSE_1TO1_55S	SENSE	CPUVCCIO80_CS_N	45 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	45
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	
	SENSE_1TO1_55S	SENSE	GPUISENS_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_N	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
	SENSE_1TO1_55S	SENSE	GPUFB_CS_P	74 99
	SENSE_1TO1_55S	SENSE	GPUFB_CS_N	74 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	98
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P	74 98
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N	74 98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	99
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	99
SENSE_DIFFPAIR_A2	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	46 66
SENSE_DIFFPAIR_A2	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	46 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_VSENSE_P	
	AUDIODIFF	AUDIO	ADC1_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_VSENSE_P	
	AUDIODIFF	AUDIO	ADC2_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_R_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_R_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_L_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_L_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_P	99
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_R_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	99

D2 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 34
	1TO1_DIFFPAIR		CHGR_CSI_R_P	61
	1TO1_DIFFPAIR		CHGR_CSI_R_N	61
	1TO1_DIFFPAIR		CHGR_CSO_R_P	61
	1TO1_DIFFPAIR		CHGR_CSO_R_N	61
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	57
B367 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_P	
B368	AUDIODIFF	AUDIO	SSM2375SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SR_P	
	AUDIODIFF	AUDIO	SSM2375SR_N	
B382 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P_R	
B383	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N_R	
B355 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 57 59
B356	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 57 59
B384 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_P	
B385	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_N	
B386 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_P	
B387	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_N	
B397 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P_R	
B398	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N_R	
B360 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 57 59
B359	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	
B392 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_P	
B393	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_N	
B394 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_P	
B395	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_N	
B402 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSUBIN_P	57
B410	DIFFPAIR	AUDIO	RSUBIN_N	57
B411 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSUBIN_P	57
B412	DIFFPAIR	AUDIO	LSUBIN_N	57
B413 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_P	
B414	DIFFPAIR	AUDIO	SSM4321SR_N	
B415 AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SL_P	
B416	DIFFPAIR	AUDIO	SSM4321SL_N	
B163 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_P	
B164 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_N	
B165 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_P	
B166 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_N	
B171 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_P	
B172 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_N	
B173 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_P	
B174	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_N	
B179 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_P	
B180	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_N	
B186 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_P	
B187	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_N	
	USB_85D	USB	USB_TPAD_R_P	26 49
	USB_85D	USB	USB_TPAD_R_N	26 49
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR	8
		GND	GND	

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15" MBP BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?

15" MBP Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_ISENSE_P	
I2		AUDIODIFF	AUDIO	ADC1_ISENSE_N	
I3	SENSE_DIFFPAIR_42	THERM_55S_CPUIMVPISNS	THERM	CPUIMVP_ISNS1_P	46 65 66
I4		THERM_55S_CPUIMVPISNS	THERM	CPUIMVP_ISNS1_N	46 66
I5	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_P	46 66
I6		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_N	46 66
I7	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_P	46 65 66
I8		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_N	46 66
I9	SENSE_DIFFPAIR	THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS3_P	46 65 66
I10		THERM_55S_CPUIMVPISNS1	THERM	CPUIMVP_ISNS3_N	46 66
I11	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_P	46
I12		THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_N	46
I13	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_P	46
I14		THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_N	46
I15	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P	80
I16		THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N	80
I17	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P	80
I18		THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N	80
I19	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_P	98
I20		THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_N	98
I21	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_P	
I22		THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_N	
I23	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_P	
I24		THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_N	
I26	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_P	39 99
I25		THERM_1TO1_55S	THERM	ISNS_SSD_N	39 99
I28	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_R_P	99
I27		THERM_1TO1_55S	THERM	ISNS_SSD_R_N	99
I30	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCHVCCIOS0_CS_P	87 99
I29		THERM_1TO1_55S	THERM	PCHVCCIOS0_CS_N	87 99
I32	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_P	87
I31		THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_N	87
I67	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P	79 80
I68	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N	79 80
I54		THERM_1TO1_55S	THERM	GPU_FBVDDQ_SENSE	73 74
I53		THERM_1TO1_55S	THERM	GPU_FBGND_SENSE	73 74
I55		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	74 79
I56		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	74 79
I33	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_P	
I34		THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_N	
I35	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_P	
I36		THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_N	
I37	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	47
I38		THERM_1TO1_55S	THERM	TBT_THERMD_N	47
I39	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	X29THMSNS_D2_P	
I40		THERM_1TO1_55S	THERM	X29THMSNS_D2_N	
I57	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_P	
I58	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_N	
I59	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_P	
I60	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_N	
I41		USB_85D	USB3	USB3_EXTA_TX_F_P	
I42		USB_85D	USB3	USB3_EXTA_TX_F_N	
I43		USB_85D	USB3	USB3_EXTA_RX_F_P	
I44		USB_85D	USB3	USB3_EXTA_RX_F_N	
I45		USB_85D	USB3	USB3_EXTA_TX_C_P	40
I46		USB_85D	USB3	USB3_EXTA_TX_C_N	40
I47		USB_85D	USB3	USB3_EXTB_TX_C_P	7 38
I48		USB_85D	USB3	USB3_EXTB_TX_C_N	7 38
I49		USB_85D	USB3	USB3_EXTB_RX_RC_P	38
I50		USB_85D	USB3	USB3_EXTB_RX_RC_N	38
I70		USB_85D	USB3	USB3_EXTA_RX_RC_P	40
I69		USB_85D	USB3	USB3_EXTA_RX_RC_N	40
I61			CLK_25M	P1V5_GPU_VSNS	
I62			CLK_25M	P1V0S0_VSNS	

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.058 MM	?
2:1_SPACING	TOP,BOTTOM	0.116 MM	?
3:1_SPACING	TOP,BOTTOM	0.174 MM	?
4:1_SPACING	TOP,BOTTOM	0.232 MM	?
5:1_SPACING	TOP,BOTTOM	0.290 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
2x_DIELECTRIC	TOP,BOTTOM	0.116 MM	?
3x_DIELECTRIC	TOP,BOTTOM	0.174 MM	?
4x_DIELECTRIC	TOP,BOTTOM	0.232 MM	?
5x_DIELECTRIC	TOP,BOTTOM	0.290 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
2x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.106 MM	?
3x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.159 MM	?
4x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.212 MM	?
5x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.265 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?
2x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.202 MM	?
3x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.303 MM	?
4x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.404 MM	?
5x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.505 MM	?

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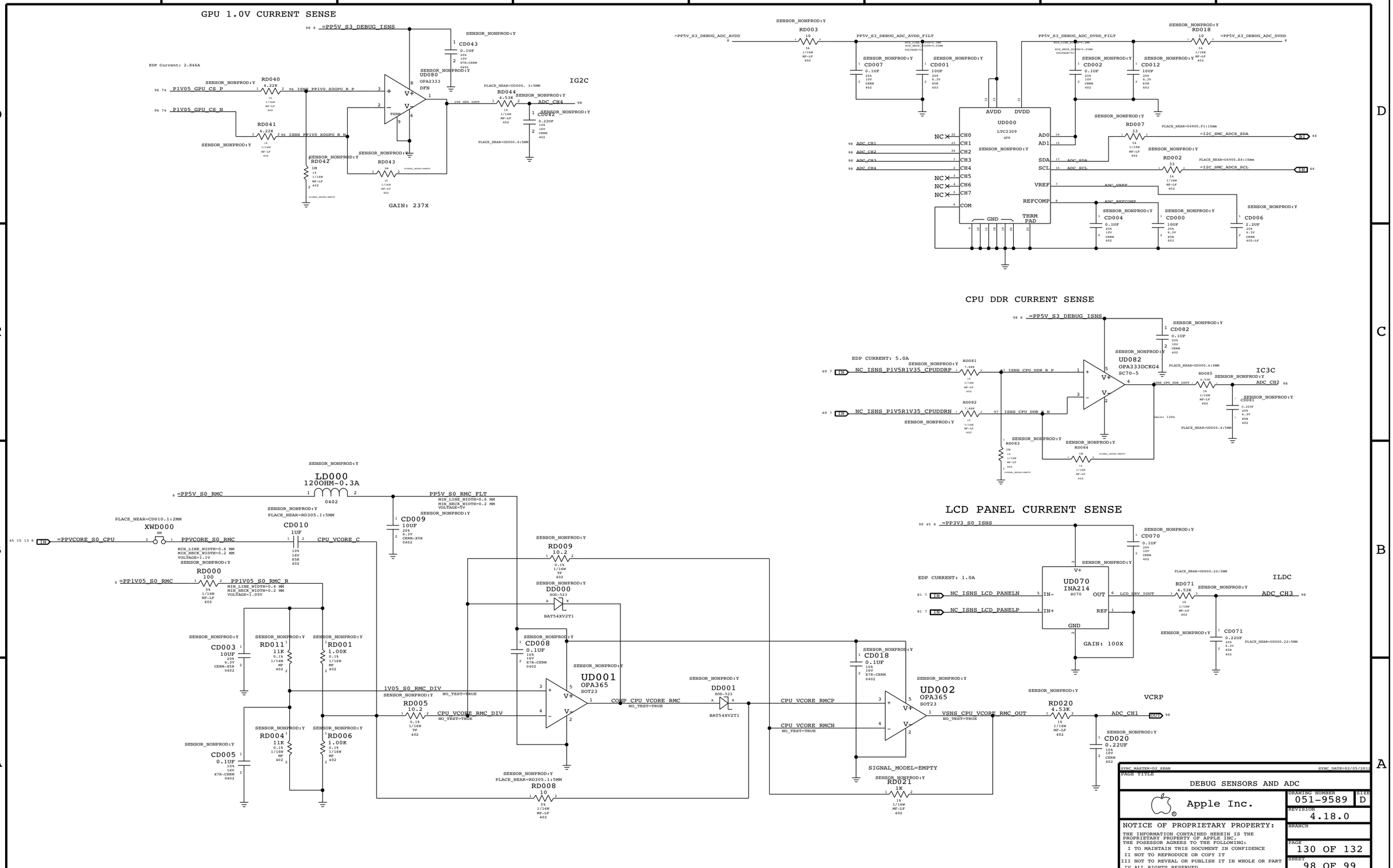
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PAGE 130 OF 132
SHEET 98 OF 99
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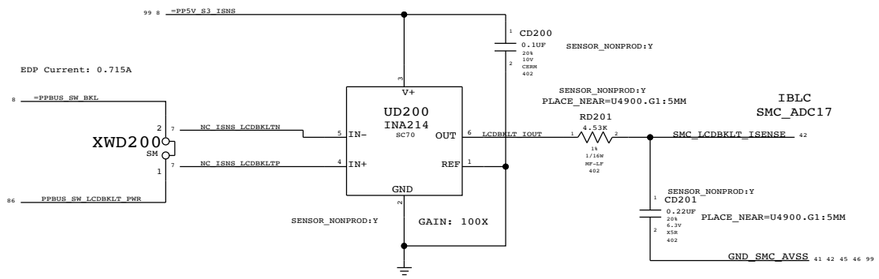
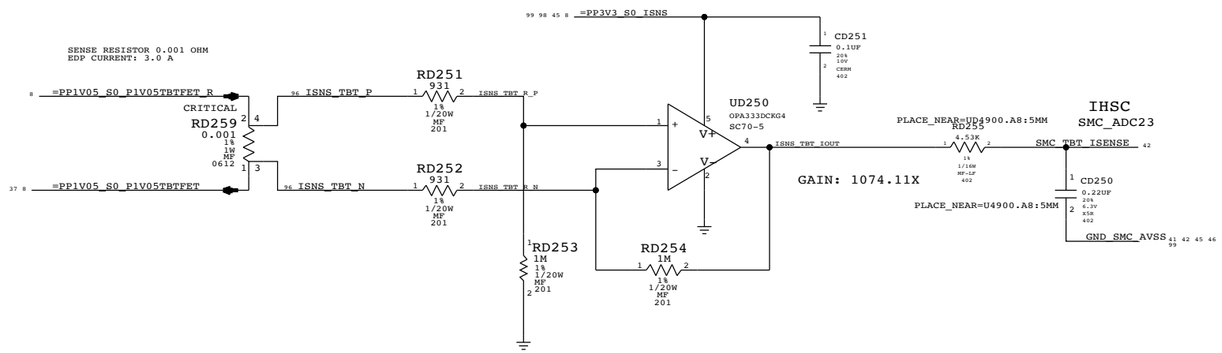
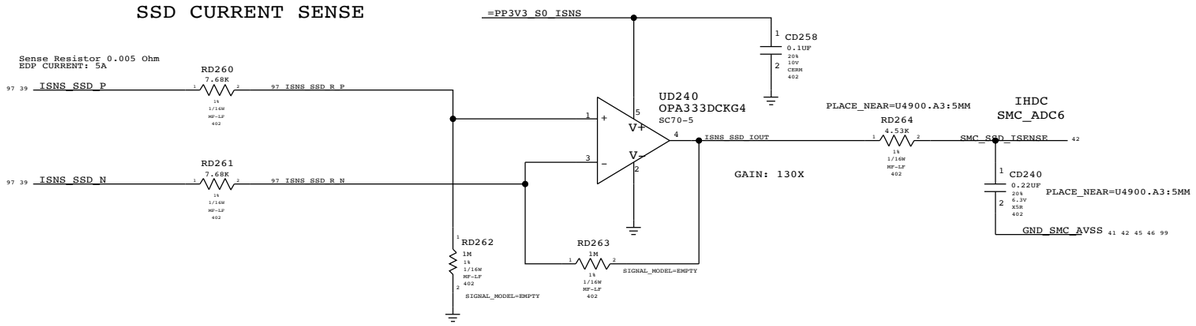
LCD BKLT Current Sense



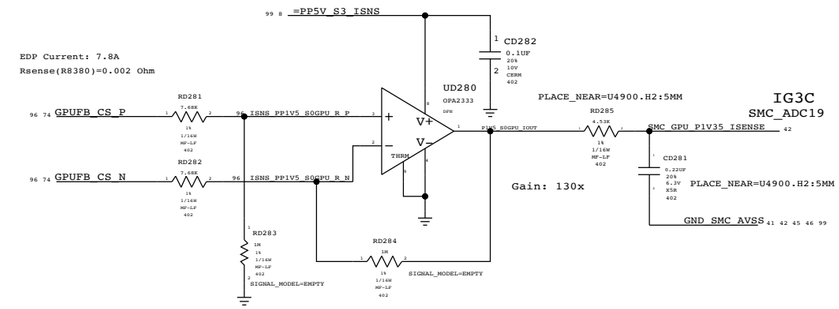
TBT (T29) CURRENT SENSE



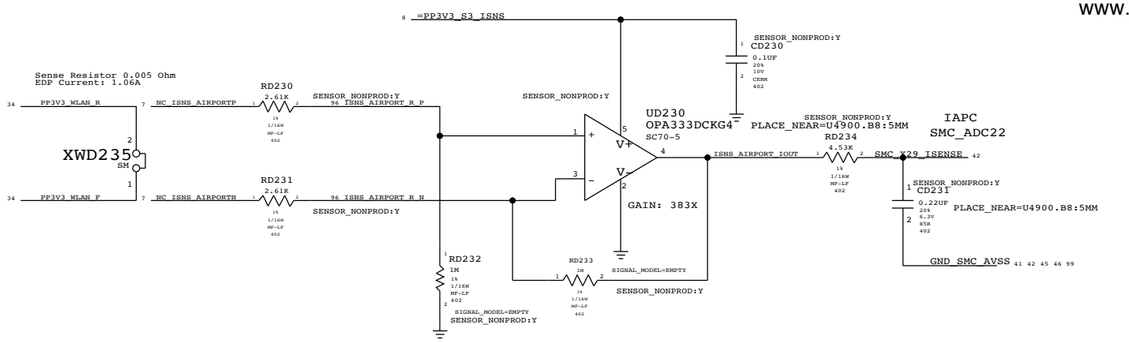
SSD CURRENT SENSE



GPU FB (1.35V/1.5V) CURRENT SENSE



X29 AIRPORT CURRENT SENSE



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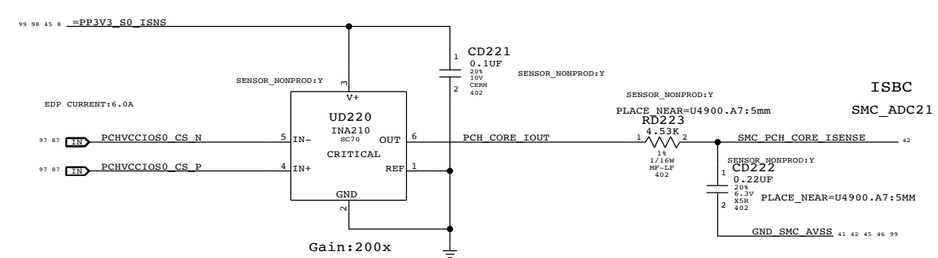
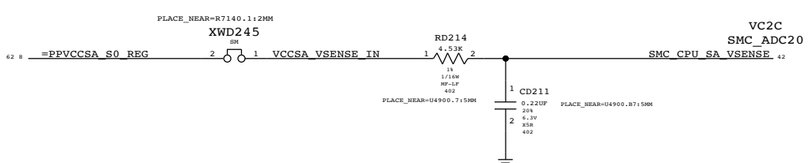
PCH VCORE CURRENT SENSE

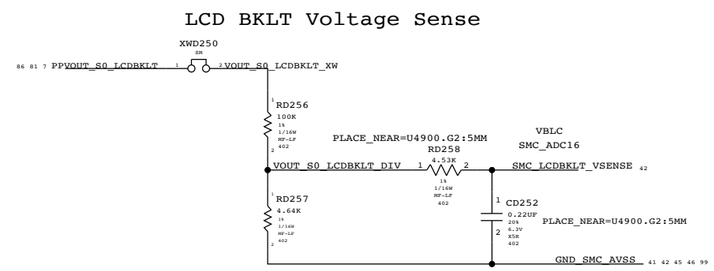


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	4	RES,MTL FILM,100K,5,1/16W,0402,SMD,LF	CD201,CD223,CD231		SENSOR_NONPROD:N

CPU VCCSA VOLTAGE SENSE



LCD BKLT Voltage Sense



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PAGE TITLE

SMC12 SENSORS EXTENDED

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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